Silicon Tungsten Calorimetry
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- Design Consideration
- Silicon Detector Design
- Electrons and Noise
- Mechanical Design

- Timing resolution
- Plans and lab activity
- Si-W Mechanical Design

Si-W work – personnel and responsibilities

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Si Detectors, Mechanical Design, Simulation

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Primary ECAL Design Requirements

- Excellent separation of $\gamma$'s from charged particles
  
  \textit{Efficiency > 95\% for energy flow}

- Good reconstruction of $\pi^{\pm}$, detection of neutral hadrons

- Reasonable EM energy resolution ($< 15\%/\sqrt{E}$)

- Reconstruct $\tau$'s and measure polarization (separate $\pi$, $\rho$, $a_1$, e's)

- Reconstruct Bhabhas and deconvolve luminosity spectra
  
  \textit{Position resolution \sim 100\mu m, bias \sim 25\mu m in endcap}
Secondary ECAL Design Requirements

- Excellent electron identification in jets (tag and b/c quarks)
- Partial reconstruction of b/c hadrons in jets
- Good $\gamma$ impact resolution for long lived SUSY neutrals
  $\sim 1 \text{ cm}$
- Good background immunity
  - Bunchlet identification
  - High granularity
SiW Design Consideration

- Transverse shower size scales with Molière radius (9mm in pure W, 16mm in pure Pb)
  ⇒ Minimize gaps between layers of absorber
  ⇒ Use a high purity W alloy

- Sample between 1/2 and 2/3 of $X_0$ (1.75mm to 2.5mm of W)

- Allow for detector segmentation at a fraction of the Molière radius
  ⇒ Use ~ 5mm pads
Si-W Calorimeter Concept

Transverse Segmentation ~5mm
30 Logitudnal Samples
Energy Resolution ~15%/E^{1/2}
Silicon Concept

- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of front end chip
- May want different pad layout in forward region
Silicon Design Details

- DC coupled detectors
- Two metal layers
- Keep Si design as simple as possible to reduce cost
- Cross talk looks small with current electronics design
Electronics Design

• Chip area driven by feedback capacitor on charge integrator and 3V supply. Need 2000 MIP (8 pC) dynamic range for 500 GeV electrons.

⇒ 10pF feedback capacitor
⇒ Effective 16 bit dynamic range

• Novel design uses two different feedback capacitors

• 5 to 10ns timing possible

• Current in input transistor pulsed duty cycle < 10⁻³

• Expect power << 40mW/wafer
Warm versus Cold Machines

• Present electronics design is optimized for a warm machine.

• In a cold machine a digital pipeline would be needed for each channel as integration over the very long bunch trains would not be possible.

⇒ Comparator presently foreseen for timing circuit could be used to trigger ADC and record bunch number

• The main impact of a cold machine would be increased power consumption and complexity in the digital portion of the chip. (The increased power consumption is a second order effect.)

⇒ Simpler warm machine electronics a good place to start
Si Prototypes

- Design completed

Provisional grid spacing for bump-bonding

6.20 $\pm$ 0.04 from pixels to a typical bump pad row

Each trace 0.006 wide

Bump Pad Array, v2.1

Detail B

Unit: mm

Traces to bump pads, typical

17.50 $\pm$ 0.04 to pixels

8/28/03

16 traces (maximum)

from pixels to a typical bump pad row

Each trace 0.006 wide

Bump Pad Array, v2.1

Detail B

Unit: mm

Traces to bump pads, typical

8/28/03

R. Frey

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Si Prototype properties – leakage current and noise

• Radiation damage to detectors is probably dominated by neutrons,
  $\sim 10 \times 10^{10} / \text{cm}^2$

  \[ \Rightarrow < 10 \text{nA} / \text{pixel leakage current} \]

• Expect typical leakage current at start of life $< 1 \text{nA/pixel}$

• Noise from leakage current at end-of-life for $1 \mu\text{s}$ sampling time (can be adjusted) and DC coupling scheme is $< 350$ electrons
• The dynamically switchable feedback capacitor scheme requires the full dynamic range only in the initial charge amplifier. ⇒ Very high power would be needed in much of the electronics chain to keep the noise floor at the equivalent of 400 electrons.

• Present design has noise:

\[ \sim 20 - 30e/\text{pf} \]

For most channels the value of \( C_{\text{input}} \) is dominated by stray capacitance of the trace connecting the pixels to the electronics:

\[ C_{\text{input}} \sim 5.7\text{pF(pixel)} + 12\text{pF(trace)} + 10\text{pF(amp)} \sim 30\text{pF} \]

\[ \longrightarrow \sim 1000 \text{ electrons noise (c.f. 24,000 from MIP)} \]
Fitting it all together

- Cartoon of possible barrel calorimeter configuration
- Assume heat flows along tungsten and/or copper heat sink to cooling water (green)
- Longest path for heat flow < 1.4m
Layout of Individual calorimeter layers:

- **Layer Assembly**: 3.6 Meters
- **Silicon**: 1.1-1.3 Meters
- **Circuit Board**: Rolled Tungsten
- **Brazed Joints**: >3.5mm

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Critical parameter: minimum space between tungsten layers.

<table>
<thead>
<tr>
<th>Config.</th>
<th>Radiation length</th>
<th>Molière Radius</th>
</tr>
</thead>
<tbody>
<tr>
<td>100% W</td>
<td>3.5mm</td>
<td>9mm</td>
</tr>
<tr>
<td>92.5% W</td>
<td>3.9mm</td>
<td>10mm</td>
</tr>
<tr>
<td>+1mm gap</td>
<td>5.5mm</td>
<td>14mm</td>
</tr>
<tr>
<td>+1mmCu</td>
<td>6.4mm</td>
<td>17mm</td>
</tr>
</tbody>
</table>

Graph showing the relationship between gap width (mm) and the angle subtended by Molière radius (mrad and deg) with and without copper heat sink.
Heat flow

Back of the envelope calculation of change in temperature:
- Thermal Conductivity of W alloy 120W/(K-m)
- Thermal Conductivity of Cu 400W/(K-m)

*Need to reduce heat to below 100mW/wafer.*

Physical model test in progress
Prototype Tungsten Pieces

- OPAL tungsten ground to size (almost more expensive than tungsten itself!)

- Prototype rolled pieces (92.5% W) look fine (some grinding still needed)

- Quality better than OPAL

- 1 m long pieces possible

- Thickness variation < 30µm
Summary of Granularity  – *Most important figure of merit*

- With 92.5% W and 1 mm gap we can have a Molière radius of

\[ \sim 14 \text{ mm} \]

which has an angular size of 11 mrad at 1.25 m

⇒ provided we can keep the power down to 40 mW wafer

- *This will be challenging, but may be possible*

What about energy resolution ⇒
• 1 GeV photons

• 0.1 $\mu$m range cuts

• 42 and 75 layers of W

• Si apparently benefits from subMIP energy deposits – can we see this in a real detector?
Toy Monte Carlo Studies of Timing Resolution for 30 Samples

Assumptions – wild guesses – (waiting for real electronics model):

- Each MIP has 30 samples at random distances from the read-out chip
- Threshold for timing measurement is 8,000 electrons.
- Input FET has $g_m = 1.5\text{mS}$ and the noise contribution from the rest of the amplifier is equal to input FET except for the "floor" noise.
- The charge measurement has a noise floor of either 0 or 4000 electrons
- Time constant for charge measurement is 200 ns.
- Time constant for the time measurement is 50 or 200 ns.
- The noise in the timing and charge circuits are uncorrelated
- Random 5% channel to channel variation in threshold
- Random 1% event-to-event variation in threshold
- Random 5% uncertainty in constants used for correction.
- Reject time measurements far from mean
Sample Timing Results
200 ns time constant, no noise floor

Time versus charge for mips

30 sample average time

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Including a 4000 electron noise floor (not needed in new electronics design):

30 sample average 200ns time constant

30 sample average time 50ns time constant

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With no noise floor (e.g., use switchable feedback capacitor) and
50ns time constant:
Practice with 6x6 1cm² cell detectors:
     Probe station

Depletion depth from CV curve

MIP with scintillator

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Si-W status

- Design of first silicon detectors complete
  ⇒ Prototypes will arrive in early '04

- Electronics design well advanced
  ⇒ Expect to be ready for submission in early '04

- Mechanical conceptual design started
  ⇒ ~ 1mm gap between layers without a copper heat sink may be possible
  ⇒ Gap size depends crucially on power consumption
Si-W Near Term Plans

• Produce prototype electronics – early next year

• Test bump bounding electronics to detectors in ’04

• Ready for Test Beam in ’05

• Confirm thermal model and explore best coupling method of chips to absorber

• Simulation job list:
  – Optimize sampling for energy resolution
  – Compare GEANT 4 /EGS and data on Eres versus silicon thickness
  – Optimize pixel layout
  – Would more granularity help?
  – How sensitive is energy flow to Molière radius?