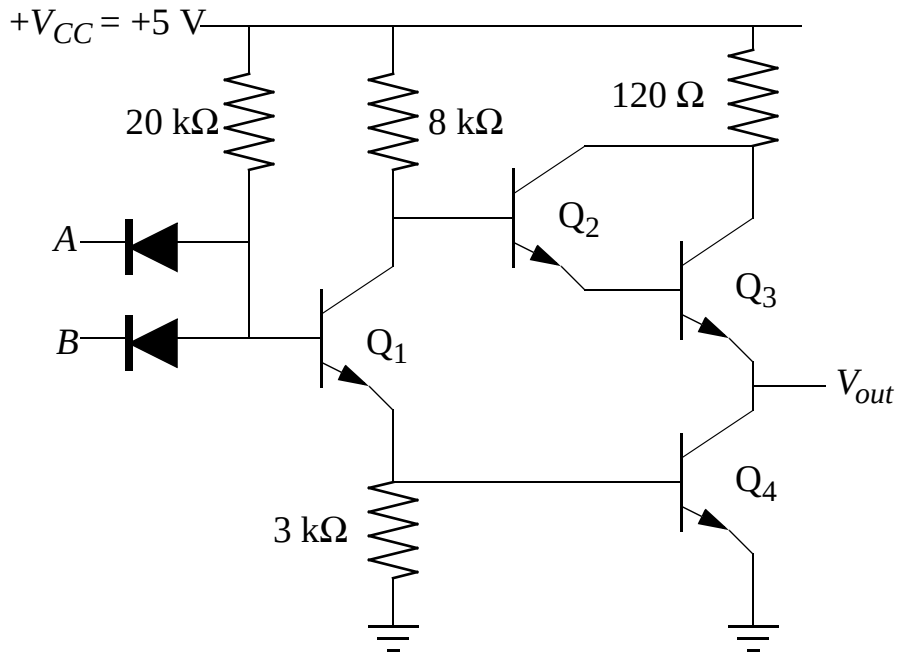
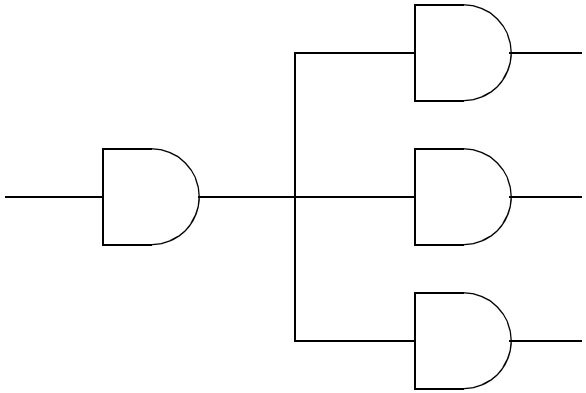
Signal Interfaces

- Circuit connections may be between digital and analog signals.
- There are also connections between different types of digital circuit element.
- The input and output charcteristics of analog and digital circuits matter.
- TTL logic sources current from the input when the input signal is low.
- It sinks current into the output when the value is low.



One Output to Many Inputs

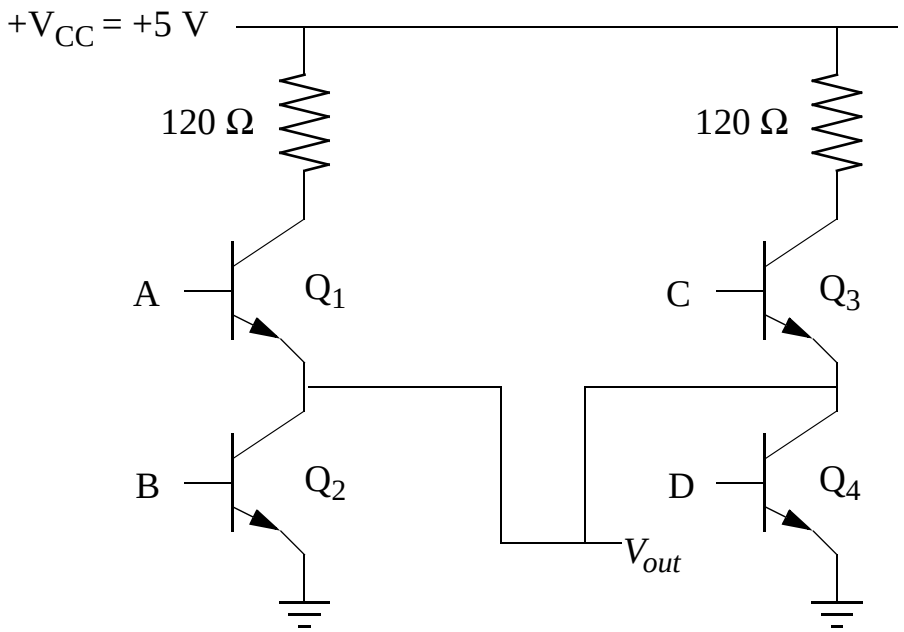
- This is the normal connection between logic gates



- TTL is limited by the imput current for LOW states, usually <8 gates.
- Buffers are used to increase the number of inputs driven by an output.

Two Outputs to One Input

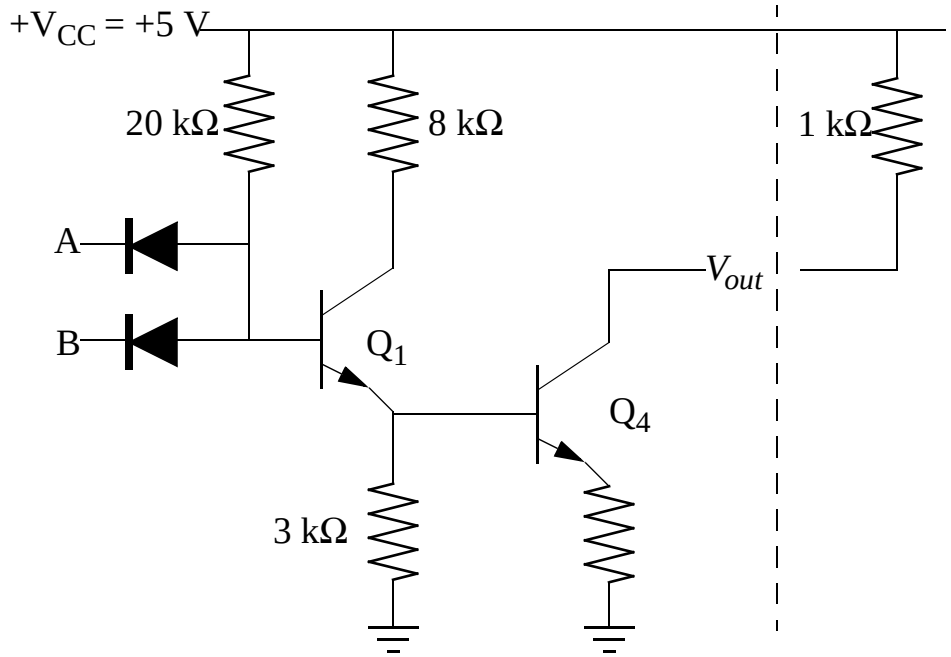
- With TTL this doesn't make sense logically or electrically.



- When the output of Q_1Q_2 is HIGH then Q_1 is on and Q_2 is off.
- When the output of Q_3Q_4 is LOW then Q_3 is off and Q_4 is on.
- If the two competing gates are connected at V_{out}, Q_4 will have a 4.3 V drop with no external resistance. Since D is at 1.4 V typically, Q_4 will be trying to draw many amps into the collector. This is likely to destroy Q_4, or if it's protected burn up the wire connecting 4.3 V to ground. between the gates.

Open Collector Logic

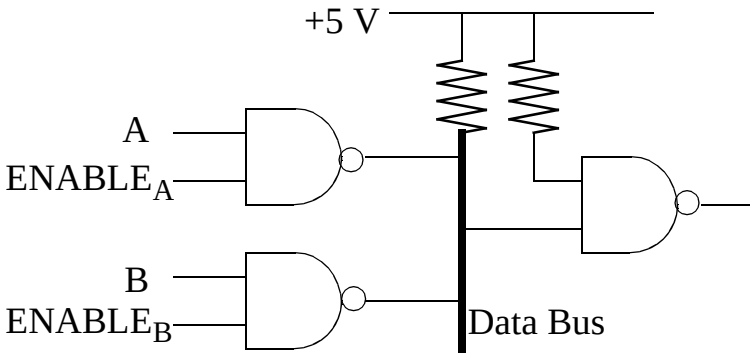
- Open collector TTL logic places the collector resistor external to the chip.



- A single resistor can be used for many chip outputs.
- Outputs are never driven high, but are pulled to +5 V externally.
- The effect is to create an AND of the outputs.

Data Bus

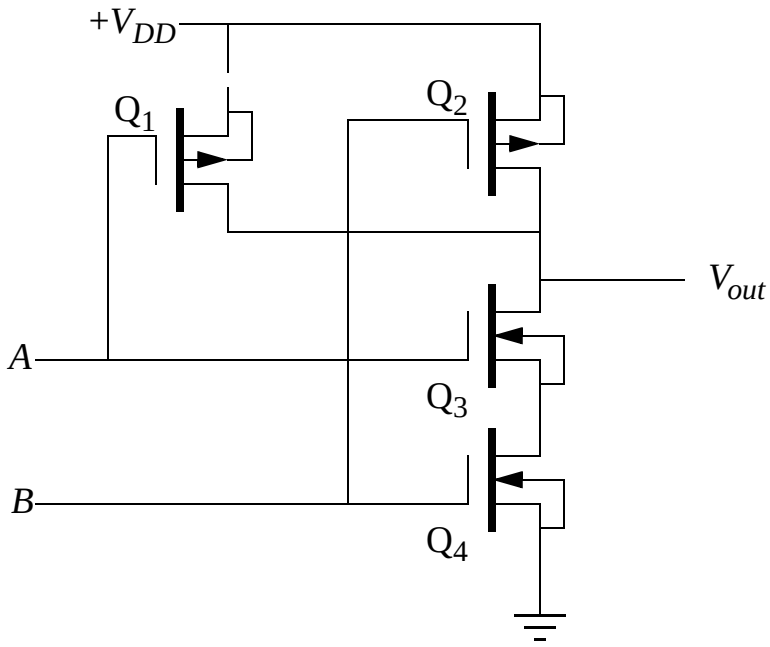
- Different gates can be switched to drive an input:



- Negative logic is frequently used to create an OR of the outputs.
- The common line used for the outputs is called a data bus.

CMOS Logic Interface

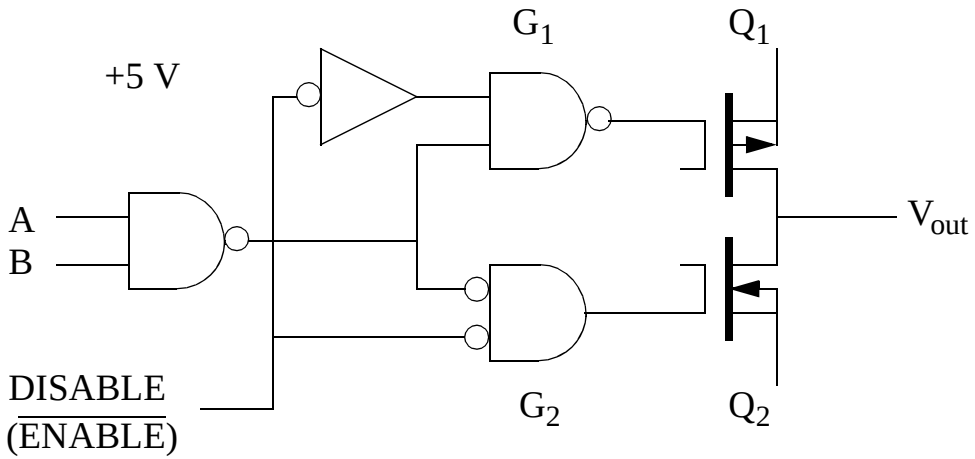
- CMOS logic has a very high impedance input that draws no current.
- The output will connet directly to the high or low voltage value.



- One CMOS ouput can drive a large number of other CMOS inputs.
- A CMOS output high tied to a CMOS output low on a bus would cause a short circuit.

Three State Logic

- CMOS logic can be controlled by an extra signal to enable or disable its output.



- If DISABLE is HIGH both AND gates G_1G_2 have one input LOW.

  The gate on Q_1 is HIGH (off).

  The gate on Q_2 is LOW (off).

  V_{out} sees an open circuit and is uninfluenced by the inputs AB.

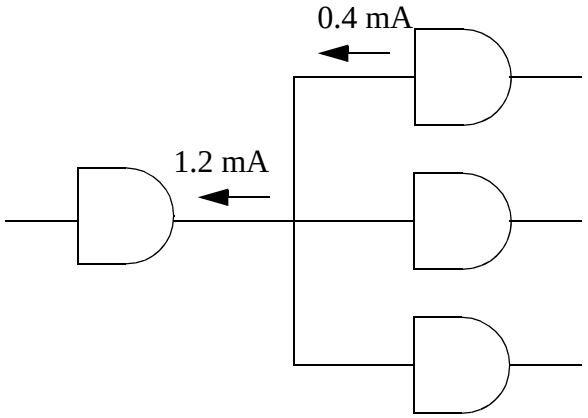
- If DISABLE is LOW both AND gates G_1G_2 have one input HIGH.

  The ouputs of gates G_1 and G_2 are both A*B and Q_1 or Q_2 will be on.

  $V_{out} = \overline{A*B}$.

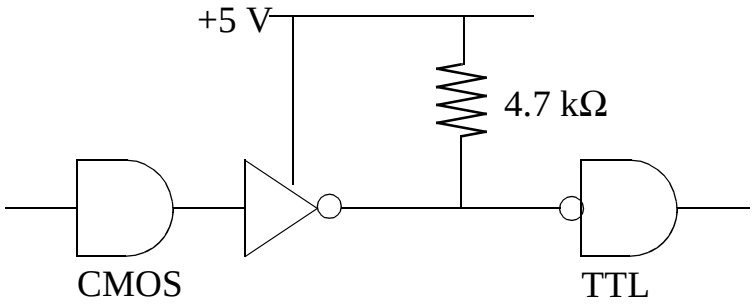
CMOS to TTL Interface

- The problem is that CMOS doesn't sink much current.



- With 500 Ω to ground this is a 0.6 V drop, and is not a good TTL LOW.

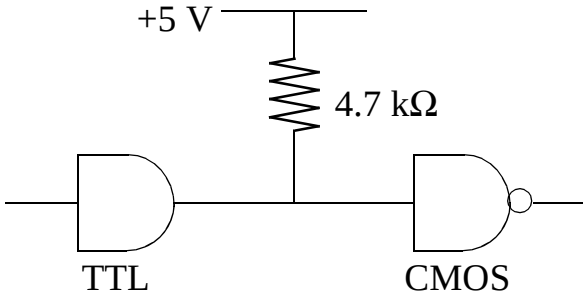
- The solution is to use a CMOS buffer or inverter.



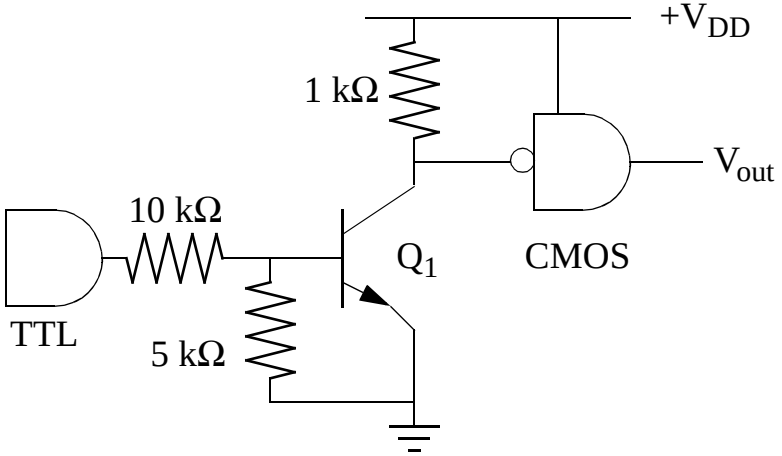
TTL to CMOS Interface

- The problem is that the output HIGH is only 3.5-4.4 V, CMOS may expect more.

- To connect with 5 V CMOS, use a pullup resistor to insure a good logic HIGH.

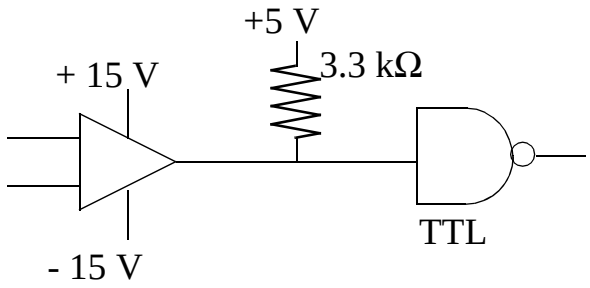


- On a logic LOW this will use about 5 mW.
- Lower values for the pullup will make the response faster at the expense of power.
- To connect to greater than 5 V CMOS, use a transistor driver or 74HCT buffer.

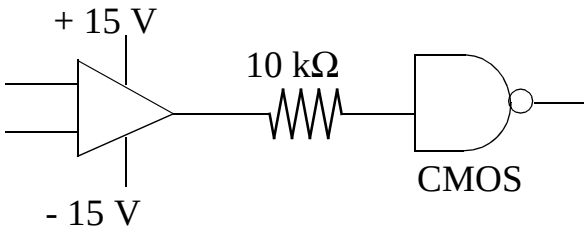


Op-Amps to Digital Logic

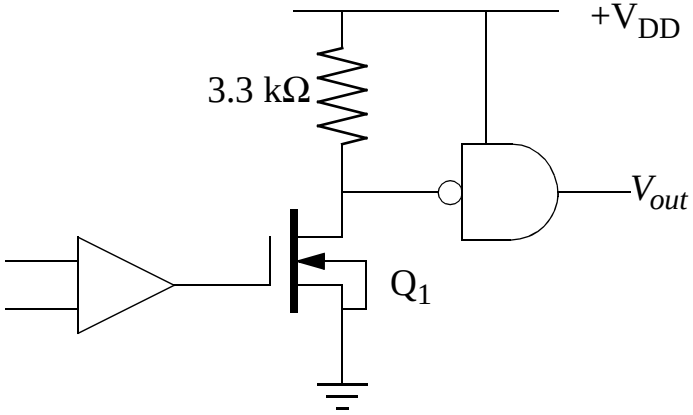
- Op-amps can be used as comparators to create a binary-valued output.
- A pullup resistor is often used with TTL to match the input requirements.



- A current-limiting resistor can be used with CMOS since the inputs are high impedance.

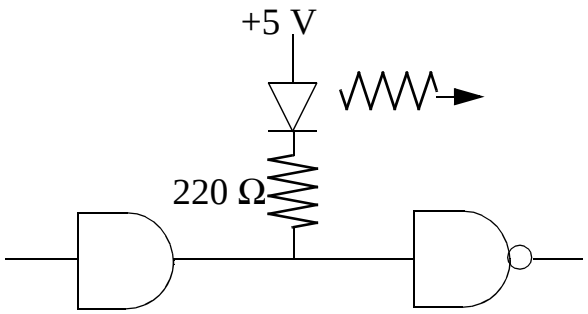


- A transistor driver insures the best match.

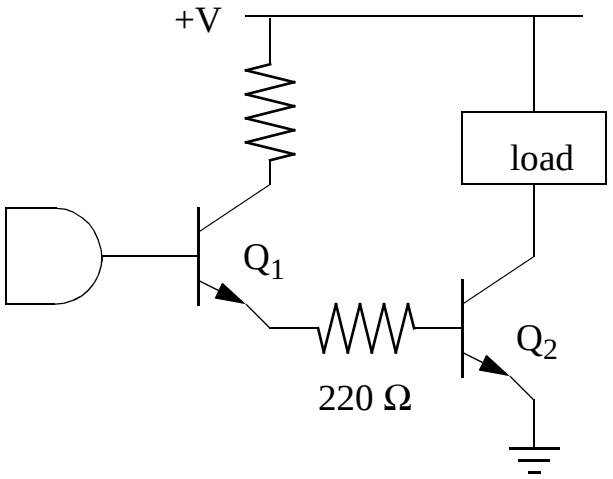


Interface to External Loads

- An LED (Light Emitting Diode) is a common load on a digital signal.
- The typical LED will turn on at 1.7 V, and 1 mA is dim, 10 mA is bright.
  TTL should sink current, CMOS can sink or source current.

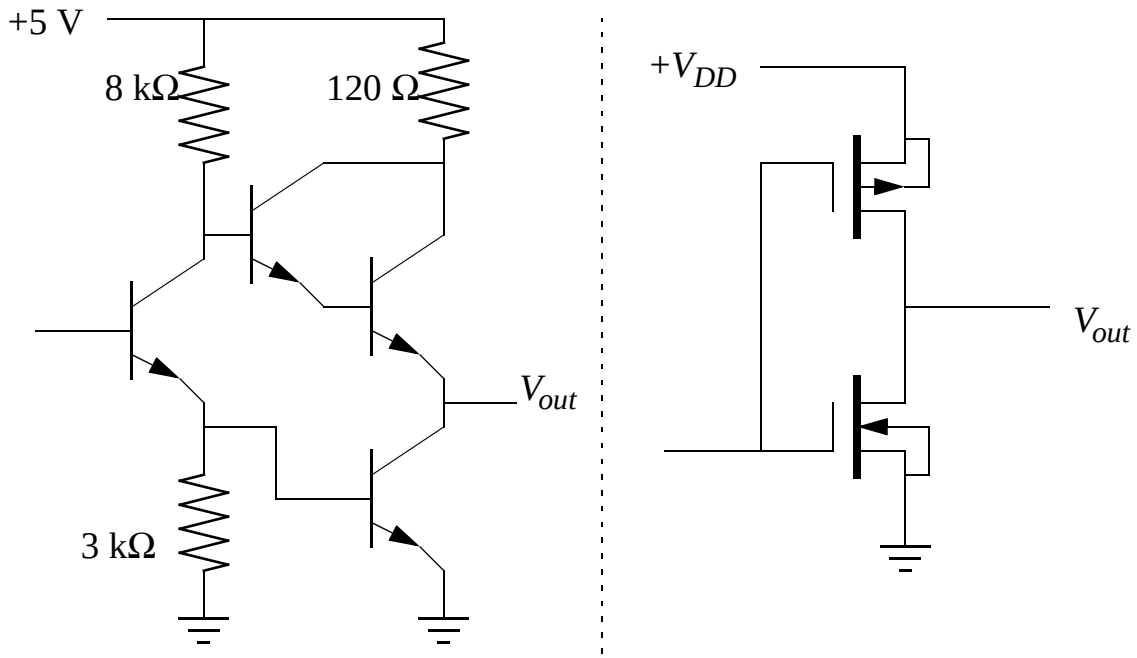


- High current loads often need a transistor driver to provide the power.



Switching Noise

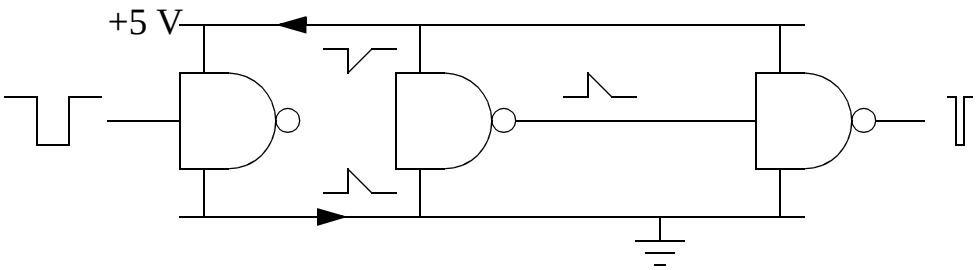
- Switching an output totem-pole for TTL or CMOS causes a brief interval (5 ns) when both transistors are on.



- The short places a negative spike on the +V line and a positive spike on the ground line.

Transient Signals

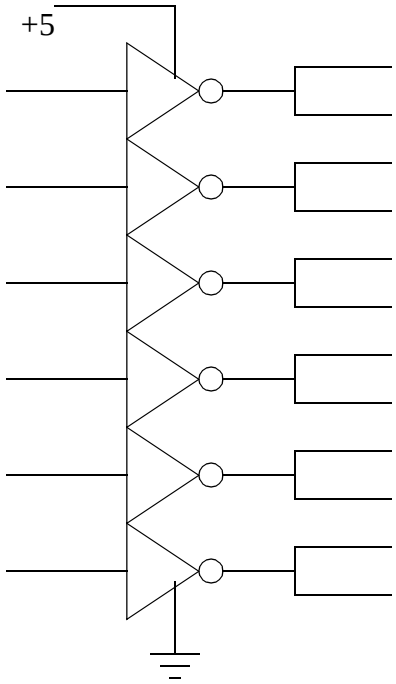
- The power or ground spike can show up on another gate.
- If the spike is sufficiently large it can possibly be interpreted as HIGH by a third gate.



- Circuit boards use large ground planes and capacitors will suppress spikes.
- Adding 0.1 μF capacitors on the power supplies near the ICs is a common technique to reduce noise.

Capacitive Loads

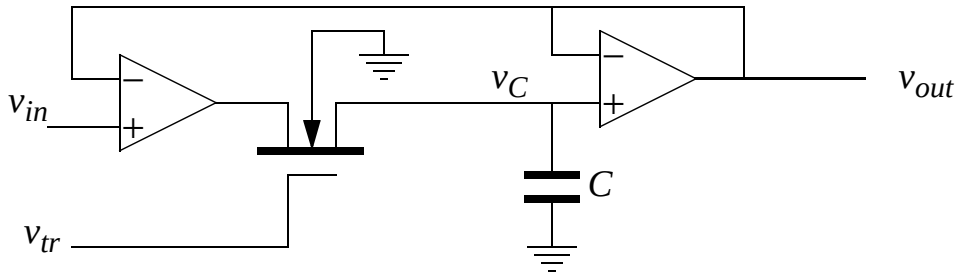
- Even with capacitors there can still be spikes. The typical wire and input capacitance is about 5 pF to ground and wire inductance is about 5nH/cm. For a fast transition $I = C(dV/dt)$ and $V = L(dI/dt)$ are important.
- Consider a hex inverter with a 2 cm wire to ground when all the inputs are making a HIGH-to-LOW transition in 2 ns.



- If each inverter is driving two other gates, the load will be 10 pF and the current will be 6(10 pF)(5V)/(2ns) = 150 mA. The voltage spike would be (10nH)(150mA)/(2ns) = 0.75 V from that one chip.

Sample and Hold

- Two x1 buffers can be combined with a MOSFET switch to create a circuit that selects voltages at specific times.



When v_{tr} = -15 V, the MOSFET is non-conducting and $v_{out} = v_C$.

When v_{tr} = +15 V, the MOSFET is conducting and $v_{out} = v_{in}$. The capacitor charges to v_{in}.

- The output current I_{out} of the first amplifier will charge the capacitor.

$$\left.\frac{dv_C}{dt}\right|_{max} = \frac{1}{C}\frac{dQ}{dt} = \frac{I_{out}}{C}$$

- The bias current I_B of the second amplifier will drain the capacitor.

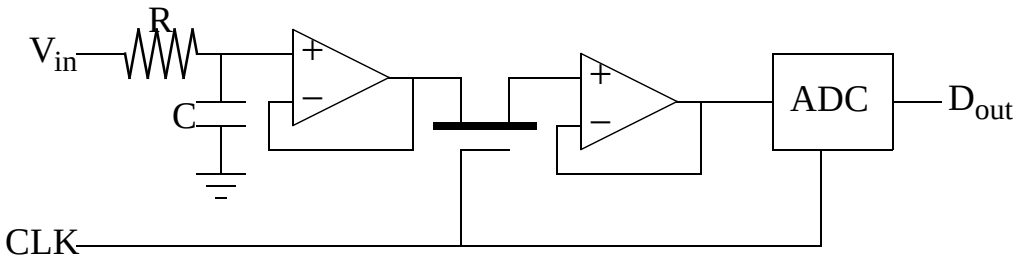
$$\left.\frac{dv_{out}}{dt}\right|_{droop} = \frac{I_B}{C}$$

- The control signal to the circuit v_{tr} is the *trigger*.

ADC with Input Filter

The sample-and-hold is an imprtant component of an digitizing circuit.

A general analog to digital conversion often includes a low pass filter before sampling.

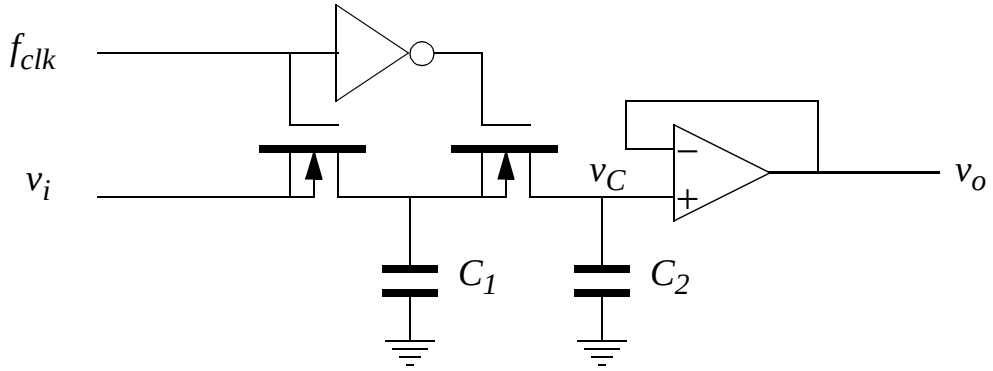


The above circuit shows the three basic parts:

1. Low pass filter
2. Sample-and-hold circuit
3. Digitizer

Switched Capacitor Filter

- Two MOSFET switches can alternately control two sample-and-hold capacitors.



When the first switch is closed $Q_1 = v_{in}/C_1$.

When the first switch is open $v_C = (Q_1+Q_2)/(C_1+C_2) = v_k$.

But Q_2 holds the voltage from the previous time $v_{k\text{-}1}$.

$$v_{ok} = \frac{C_1}{C_1 + C_2} v_{ik} + \frac{C_2}{C_1 + C_2} v_{ok-1}$$

- This is a *recursive* filter

It can be shown that $\omega_B = f_{clk} \ln\left(1 + \frac{C_2}{C_1}\right)$

The filter depends on the digital clock frequency.