Analog to Digital

Conversion from analog to digital values is more complicated than digital-to-analog.

- A digital value is precise to its least significant bit.
- An analog value has a precision set by the measurement. The digitization becomes the precision of the measurement.

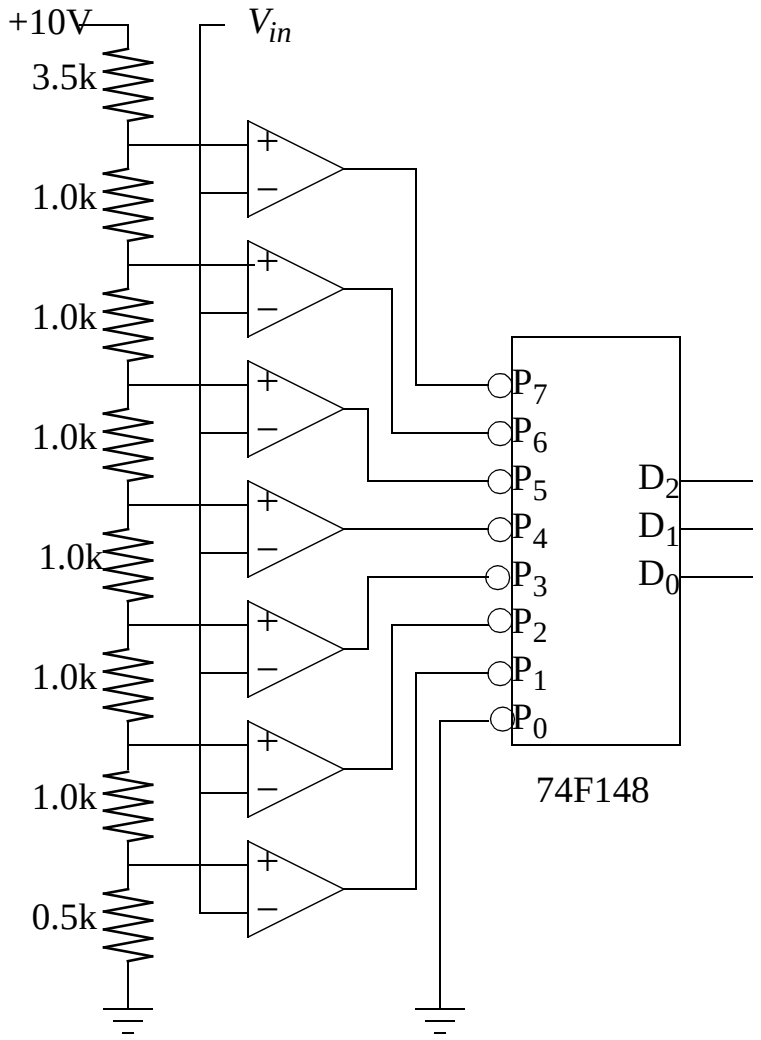
- Digital values typically change only at well defined intervals determined by a clock.
- Analog values may change at significant or insignificant rates based on the circuit and environment. Digitization captures a snapshot of the analog value.

Parallel Encoder

- The simplest design for an ADC is a series of comparators set to different thresholds.

- A voltage divider sets up a sequence of predefined thresholds.
- Comparators indicate which of the thresholds have been exceeded.
- An encoder converts the comparators output to a 3-bit digital value.

- In the example the thresholds are at 0.5 to 6.5 V in steps of 1.0 V.
- The output bits represent the voltage to the nearest whole volt.



Flash ADC

- The parallel encoder is an example of a *flash* ADC.

  The name comes from the very fast conversion from analog to digital.

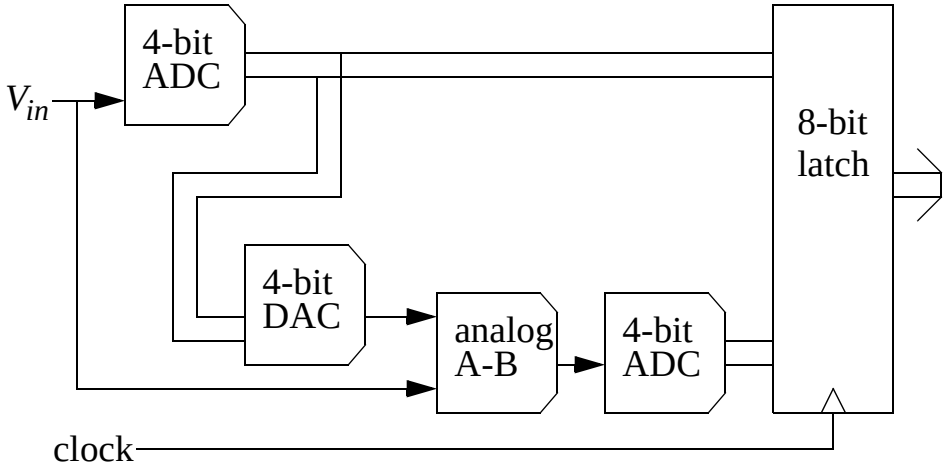
- The 3-bit example shown has no clock and converts as soon as the V_{in} changes, limited by the speed of the comparators and priority encoder (74F148).

- In general a flash ADC would have a clock controlling an output enable to a latch, so that the digital values would only change at set times.

- Flash ADCs require one comparator for each value.
- An 8-bit ADC would require 256 separate comparators with separate voltage settings.
- The number of comparators increases exponentially with the number of bits of precision.

Half-flash ADC

- At the cost of some speed a *half-flash* ADC can be constructed from two smaller flash ADCs.



1. The input voltage is digitized by a coarse ADC filling bits 4-7.
2. The output is converted back to an analog value.
3. The converted value is subtracted from the original voltage forming an analog remainder.
4. The remainder is digitized by a fine ADC filling bits 0-3.
5. An external clock controls the latch insuring all steps are completed before the output is updated.

Sampling Errors

Once a clock establishes a sampling time T there are errors that can occur in the digitization. The two possibilities are:

1. The sampling time is too slow.

   The changes in analog values will be missed in the digital values. Ideally every change in the input signal that is at the level of the LSB should be captured by the digital output. For slowly changing signals maximum slope (s in V/s) sets the needed sampling time.

$$T < \frac{V_{LSB}}{s}$$

2. The sampling time is too fast.

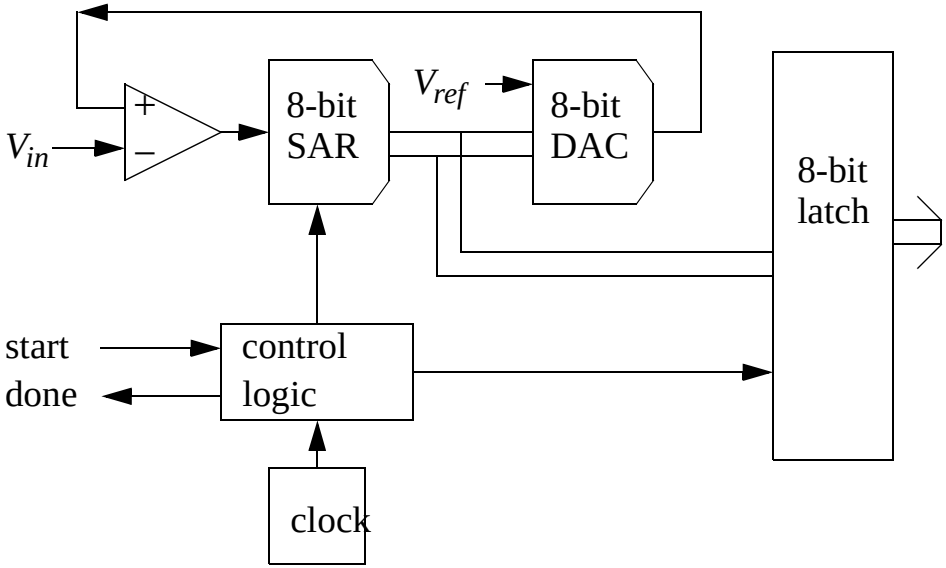
   If the sampling time is fast compared to noise on the input signal, and the noise is of a magnitude greater than the LSB it will be preserved and possibly enhanced by the digitization process. Too avoid senistivity to noise (with frequency f_N), it needs to be filtered, or set the sampling time to a larger value.

$$T > \frac{1}{f_N}$$

Successive Approximation ADC

- A successive approximation ADC extends the idea of a half flash ADC to the single bit using only one comparator.
- The basic units of a successive approximation ADC are:

1. Comparator - Compares the input analog value to the current approximation.
2. Succesive Approximation Register (SAR) - The SAR starts with 1 in the MSB and 0 for all other bits. With each clock input the SAR resets the current bit if the comparator is HIGH and moves to the next bit down by setting it.
3. DAC - Converts the bit pattern from the SAR into an analog value for the comparator.
4. Latch - Stores the bit pattern when the LSB is complete.
5. Control Logic - Counts n clock pulses to the SAR then sends DONE to the latch.



Sequence Example

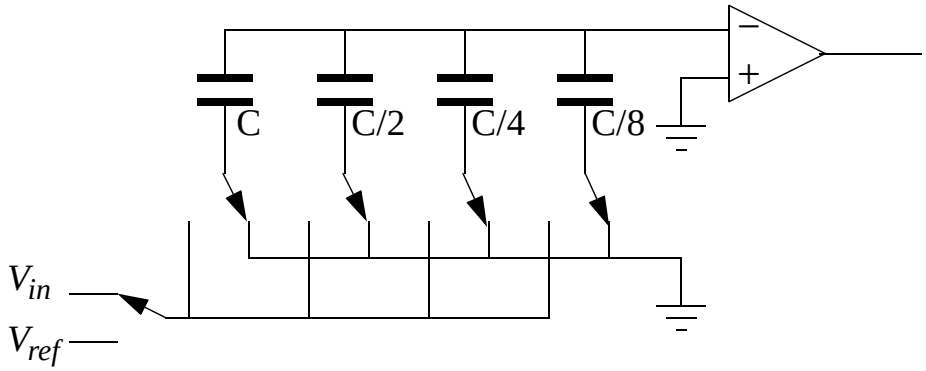
For an 8 bit ADC set V_{ref} to 5.12 V so the LSB is set to 20 mV.

Clock	SAR	DAC
START	10000000	2.56 V
CLK 1	11000000	3.84 V
CLK 2	10100000	3.20 V
CLK 3	10010000	2.88 V
CLK 4	10011000	3.04 V
CLK 5	10010100	2.96 V
CLK 6	10010110	3.00 V
CLK 7	10010111	3.02 V
DONE	10010110	3.00 V

The process takes 8 clock cycles to get a result. For a 1 MHz clock this would result in a digitization time of 8 µs. This would require a DAC that could convert in less than 1 µs.

Switched Capacitor ADC

- It is common to use an array of capacitors to provide the digital control.

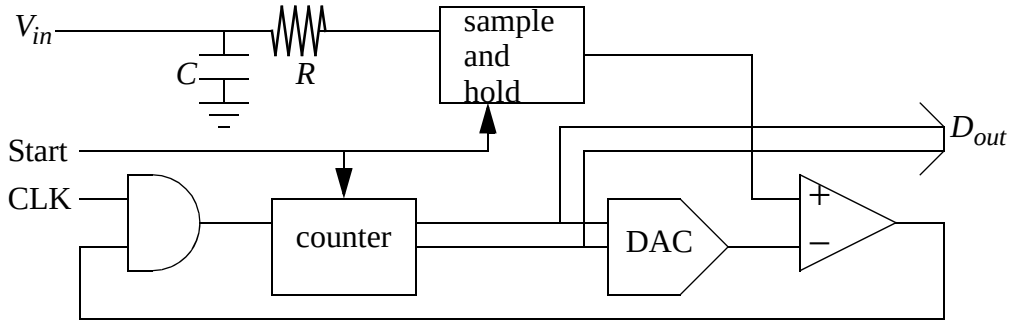


1. The capacitor array is discharged to ground.
2. All capacitors within the array are switched to the input signal, V_{in}. The capacitors now have a charge equal to their respective capacitance times the input voltage. $Q_i = V_{in}C/2^i$.
3. The capacitors are then switched to ground so that the charge at the comparator's input is $-V_{in}$.
4. The MSB capacitor is switched to V_{ref}, which corresponds to the full-scale range of the ADC. The MSB capacitor forms a 1:1 divided between it and the rest of the array, and the input voltage to the comparator is now $-V_{in} + V_{ref}/2$.
5. If V_{in} is greater than $V_{ref}/2$ then the comparator outputs a digital 1 as the MSB, otherwise it outputs a digital 0 as the MSB.
6. Each capacitor is tested in the same manner as the comparator input voltage converges to zero.

Counter ADC

- An ADC can be built from a clock, a counter, a DAC and a comparator.

1. An external start signal resets the counter and operates the sample-and-hold circuit.
2. The output of the counter is converted into an analog value by a DAC.
3. When the DAC output matches the input voltage, the clock is stopped and the digital value is read out.



- The circuit is only as fast as the time it takes for the counter to reach full scale: $2^n T_c$.
- The output will be as precise as the DAC that is used by the comparator.
- The DAC must be faster than the clock.

Integrating ADC

- An integrating ADC also uses a clock-counter combination to measure the charging time of a capacitor compared to a reference value.

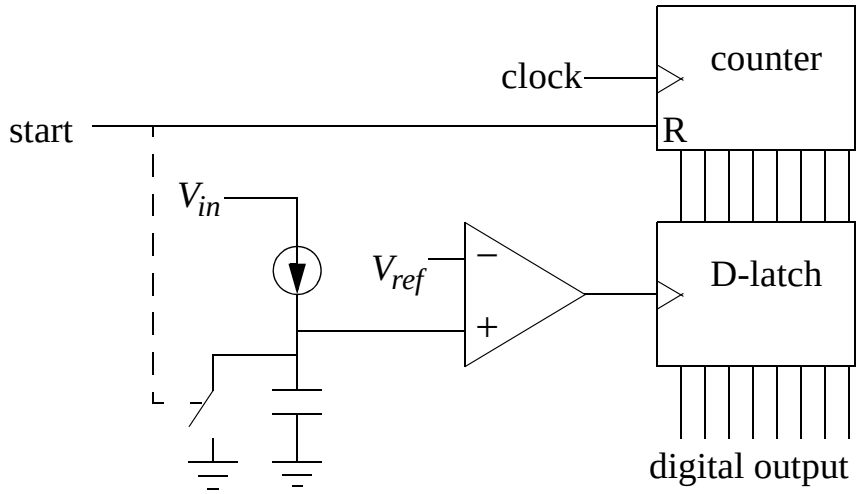
1. Convert the input voltage into a current. $I_{in} = aV_{in}$ (a is a constant).
2. Use the current to charge a capacitor yielding a time inversely proportional to the input voltage.
3. Measure the time with a digital counter operated at a fixed clock frequency.

$$CV_{ref} = Q$$

$$CV_{ref} = I_{in}\Delta T$$

$$CV_{ref} = aV_{in}\Delta T$$

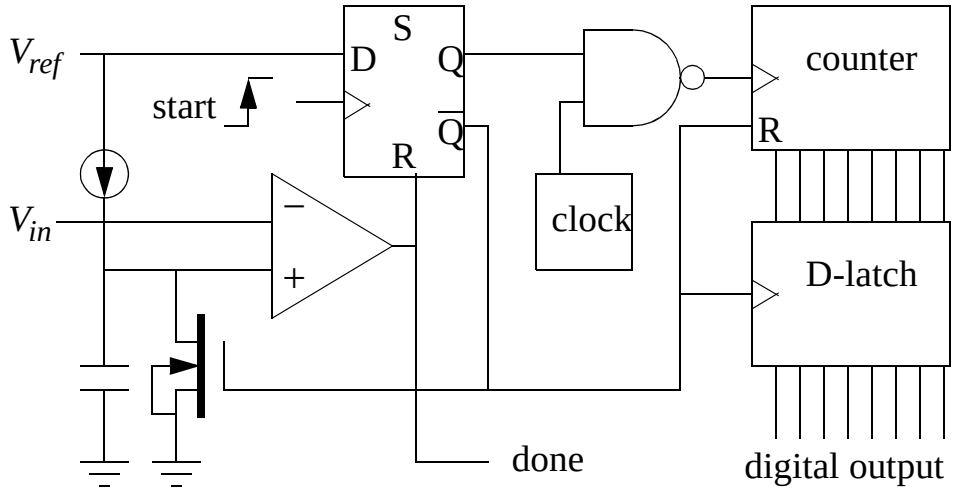
$$V_{in} = \frac{CV_{ref}}{a\Delta T}$$



- The time can be measured as the capacitor charges, discharges or both. In this example the digital value would be inverted to get a value linear with the input.

Single Slope Integration

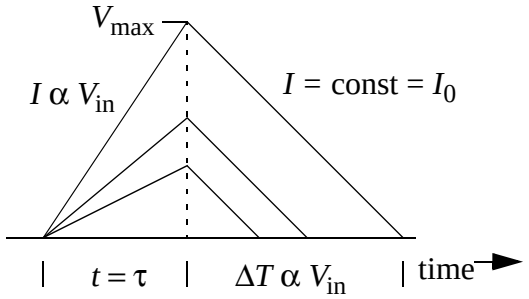
- If the reference voltage is integrated then the time becomes linear with the input voltage.
- Single slope integration relies on the stability of the capacitor and comparator to get an accurate reading.



1. A start pulse clocks a D-flip-flop causing it to go HIGH and allowing the clock to increment a counter.
2. The $\overline{Q}$ output of the flip-flop turns off an FET and the capacitor begins a linear ramp for $t = CV/I$.
3. At that time the comparator goes HIGH and resets the flip-flop, latching the counter output and signalling the end of the digitization.
4. The reset also clears the counter and discharges the capacitor through the FET.

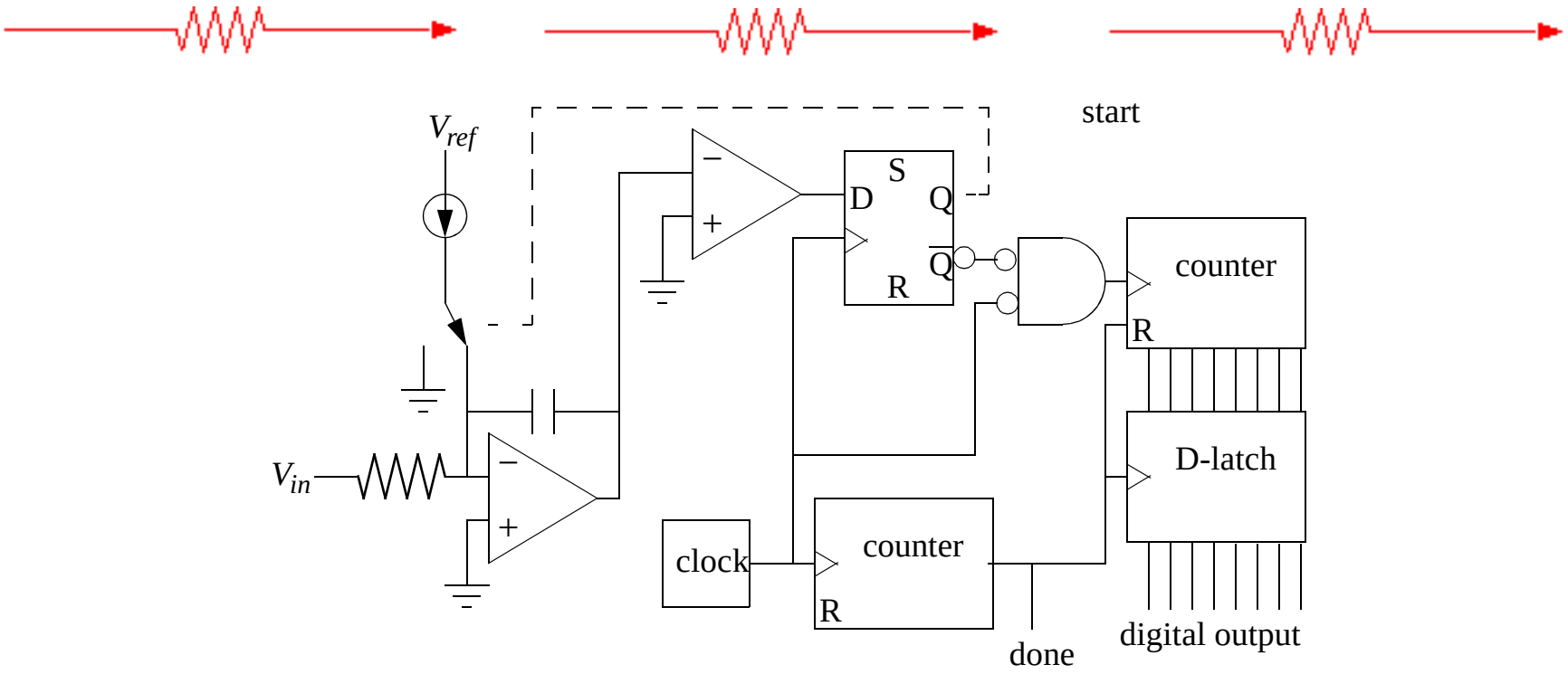
Dual Slope Integration

- One solution to the strict requirements on a single slope-integrator is to use the capacitor for both the reference and signal integration so that the effects of the capacitor cancel on the two measurements. This is called *charge-balancing*.
- Charge balancing also eliminates external noise by integrating over a longer time and letting any noise be averaged out.



- Dual slope integration charges the capacitor for a fixed time from a current source set by the input voltage; $V_{max} = I_{in}\tau/C$.
- The same capacitor is discharged with a constant current sink that is measured with a counter; $\Delta T = V_{max}C/I_0$.
- The measured time is then $\Delta T = I_{in}\tau/I_0$.
- If the same clock is used for both slopes, any variation in clock period is also cancelled out.

Delta-Sigma Converter



1. The integrating op-amp sums current from both V_{in} (negative) and the current source.
2. The output of the integrator is compared to ground, and if it is lower the flip-flop goes LOW and switches off the current source and the intgrator output rises from V_{in}.
3. One counter is always counting and the other only counts when the current source is on.
4. When the fixed counter is done, the digital output measures a count that is proportional to the current pulled from the source, and hence proportional to the input voltage.

Voltage to Frequency ADC

- Analog control is sometimes needed to generate a fixed frequency.
- One such circuit is based on an integrating ADC, but uses the counter as an oscillator.

1. A capacitor discharges at a fixed threshold.
2. The oscillator has a frequency proportional to the charging rate.
3. The frequency is proportional to the input voltage.