## Digital to Analog



- A digital-to-analog converter (DAC) takes a set of binary levels and creates a single analog value.
- The simplest DACs are derived from opamp summing circuits with different amplification ratios for different bits.
- The circuit at right requires a scaled resistor set.


For $D_{n}=0$ or 1 , where 1 is set to $\mathrm{V}_{\mathrm{CC}}$, the output will be:

$$
V_{\text {out }}=\frac{V_{C C} R_{2}}{R_{1}}\left(\frac{D_{3}}{1}+\frac{D_{2}}{2}+\frac{D_{1}}{4}+\frac{D_{0}}{8}\right)
$$

For $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{R}_{2}=1 \mathrm{k} \Omega$, and $\mathrm{R}_{1}=1.25 \mathrm{k} \Omega$ the four indiviual resistors for the inputs would be 1.25 k , $2.5 \mathrm{k}, 5 \mathrm{k}$ and $10 \mathrm{k} \Omega$. The nominal step between input values $(\mathrm{LSB})$ is 0.5 V . The maximum $\mathrm{V}_{\text {out }}=$ 7.5 V.

## Output Errors



- There are specific types of errors that can arise from a DAC such as a summing junction.
- The dynamic range may be insufficient.
- For a large number of bits one needs a large range of resistors.
- The amplifier must be able to drive the full range.
- For 16 bits this is a range of over 64000 from the lowest to highest possible value with accuracy and sensitivity appropriate at all scales.


## Scaling Errors



- There are also error types associated with DACs with sufficient dynamic range.
- Nonmonotonic behavior

For instance, let the 4-bit example above have input resistors with $10 \%$ tolerance. Within tolerance it is possible that these resistors are actually $1.37 \mathrm{k}, 2.25 \mathrm{k}, 4.5 \mathrm{k}$ and 9 k . For a digital input of 7 , the output voltage is $5 \mathrm{~V}^{*} 1 \mathrm{k} \Omega /(1 / 2.25 \mathrm{k} \Omega+1 / 4.5 \mathrm{k} \Omega+1 / 9 \mathrm{k} \Omega)=3.89 \mathrm{~V}$. For a digital input of 8 , the output voltage is $5 \mathrm{~V} * 1 \mathrm{k} \Omega / 1.37 \mathrm{k} \Omega=3.65 \mathrm{~V}$, an output lower than the one for 7 .

- Nonlinear behavior

Similar to nonmonotonic errors, but the errors in the resistors are not large enough to cause one output value to be lower than the preceding one. An example from above would be to replace the $1.37 \mathrm{k} \Omega$ resistor with a $1.25 \mathrm{k} \Omega$ resistor. Inputs 6,7 and 8 now give outputs of $3.33 \mathrm{~V}, 3.89 \mathrm{~V}$ and 4.00 V respectively. The steps of 0.56 V and 0.11 V are far from equal.

- Scale error

If in the 4-bit example the only error was that $\mathrm{R}_{2}=1.04 \mathrm{k} \Omega$. The steps would all be equal at 0.52 V . Full scale would be 7.8 V instead of 7.5 V .

## R-2R Ladder



- The $R-2 R$ ladder converts binary bits to scaled currents.

- The equivalent resistance between $V_{r e f}$ and ground is $R$, regardless of the switches, since the opamp will hold the non-inverting input to ground as well.
- Half the current from $V_{\text {ref }}$ goes towards $D_{3}, 1 / 4$ goes towards $D_{2}, 1 / 8$ goes towards $D_{1}$, and $1 / 16$ goes towards $D_{0}$. The op-amp sums the input currents and multiplies them times $R_{f}$ to get $V_{\text {out }}$.
- An analog switch would be needed to convert binary signals into switch controls.
- Note that only two resistor values are needed.


## Current Switch ICs



- These chips use the $R-2 R$ ladder design directly with transistors to make an analog current proportional to the binary number input.


Note: the line through the bases connects all the bases to the op-amp output.

- The op-amp will hold the non-inverting input to ground drawing a current from $I_{r e f}=V_{r e f} / R_{0}$. That current flows into the collector of the transistor and the op-amp will hold the base such that $I_{C}=$ $I_{r e f}$. That means that $V_{E^{-}} V_{-}=I_{r e f} R$.
- The voltage at all the emitters will be the same and the $R-2 R$ ladder will again cause each transistor in line to draw half the current of the preceding one.


## Analog Current Switches



- Consider a DAC with 1 mA full scale output.

- The capacitor eliminates switching noise and a $100 \Omega$ resistor will convert the 1 mA to 100 mV .
- Op-amps can also be used to drive the output voltage.

- $V_{\text {out }}$ at full scale equals 10 V .


## Time Averaging Converters



- Instead of summing voltage or currents, counters can be used to generate a frequency. The digital pulses can be averaged using a low-pass filter to get a voltage.
- A frequency-to-voltage converter uses a counter to feed into a low pass filter.
- To avoid nonlinearity, $R C$ must be long enough for the output to settle.
- Ideally $\mathrm{RC}>0.69(n+1) T_{0}$, where $n$ is the number of bits and $T_{0}$ is the input clock period.
- The averaged rate multiplier is a slow form of frequency-to-voltage converter useful in temperature control.



## Pulse-width Modulation



- This is similar to the frequency to voltage converter, but the counter controls pulse width instead of frequency.

- Instead of a preset to the counter, a magnitude comparator is used to vary pulse width.
- Like the frequency to voltage converter, this is slow due to the $R C$ time constant.
- It is very useful for slow loads, particularly mechanical systems or systems like thermostats.


## Modulation with a Timer



- A mechanical tachometer can be built from a 555-timer.

- The zener diodes and capacitor protect against over voltage spikes from the engine.
- The capacitor and resistor divider on the TRG input bias the input pulse to match the threshold of the 555.
- The 555 timer is used as a monostable multivibrator, with a pulse width equal to $T=R C$.
- The ammeter is slow, and used as a voltage averaging device.
- The output will be high for a fraction of time equal to $T f$, where $f$ is the frequency of input pulses.


## Johnson Counter



- A johnson counter, also called a twisted ring counter is a shift register with feedback.

- The inverse of the last output is fed back to the first input.
- The latch outputs go into a summing amplifier.
- If all resistors are equal, then the output is the sum of the 1 's in the counter at one time.


## Johnson counter truth table

| $m$ |  |  |  |  | $q$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| count | $\mathrm{Q}_{0}$ | $\mathrm{Q}_{1}$ | $\mathrm{Q}_{2}$ | $\mathrm{Q}_{3}$ | $\mathrm{Q}_{4}$ | $\mathrm{Q}_{5}$ | $\mathrm{Q}_{6}$ | $\mathrm{Q}_{7}$ | out |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| 3 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 3 |
| 4 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 4 |
| 5 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 5 |
| 6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 6 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7 |
| 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7 |
| 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 6 |
| 10 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 5 |
| 11 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 4 |
| 12 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 3 |
| 13 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 2 |
| 14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The period $T$ is 16 times the clock period $\tau$, the frequency is $1 / 16$ the clock frequency.

## Digital Wave Generation



- The resistors in the Johnson counter need not be equal.
- Different value can make different shaped waveforms.
- To get a specific wave the signal can be broken down with Fourier analysis.
- For instance, one can simulate a sine wave.
- The period can be written in terms of the Johnson clock period.
- Use $\omega=2 \pi / \mathrm{T}=\pi / 8 \tau$

$$
v(t)=\frac{a_{0}}{2}+\sum_{n=1}^{\infty}\left[a_{n} \cos (n \omega t)+b_{n} \sin (n \omega t)\right]
$$

For an even wave the $b_{n}=0$.

- The Fourier coefficients are

$$
a_{n}=\frac{1}{8 \tau} \int_{-8 \tau}^{8 \tau} v(t) \cos \left(\frac{n \pi t}{8 \tau}\right) d t=\frac{1}{4 \tau} \int_{0}^{8 \tau} v(t) \cos \left(\frac{n \pi t}{8 \tau}\right) d t
$$

## Seven-bit Sine Wave



- The $v(t)$ are quantized in steps $v_{1} \ldots v_{7}$.
- From symmetry, these can be reduced to 4 separate values.

$$
\begin{gathered}
A=v_{1}=v_{7}-v_{6} \quad B=v_{2}-v_{1}=v_{6}-v_{5} \\
C=v_{3}-v_{2}=v_{5}-v_{4} \quad D=v_{4}-v_{3} \\
a_{n}=\frac{2}{\pi n}\left[2 A \sin \left(\frac{\pi n}{8}\right)+2 B \sin \left(\frac{2 \pi n}{8}\right)+2 C \sin \left(\frac{3 \pi n}{8}\right)+D \sin \left(\frac{4 \pi n}{8}\right)\right]
\end{gathered}
$$

- Solve to minimize the higher order harmonics, $a_{3}=a_{4}=a_{5}=0$.

$$
\begin{aligned}
& A=0.150, B=0.278, C=0.363, D=0.392 \\
& \text { If } R_{4}=R_{\mathrm{f}}=10 \mathrm{~K} \Omega, \\
& R_{1}=R_{7}=26.1 \mathrm{~K} \Omega, \quad R_{2}=R_{6}=14.1 \mathrm{~K} \Omega, \quad R_{3}=R_{5}=10.8 \mathrm{~K} \Omega .
\end{aligned}
$$

