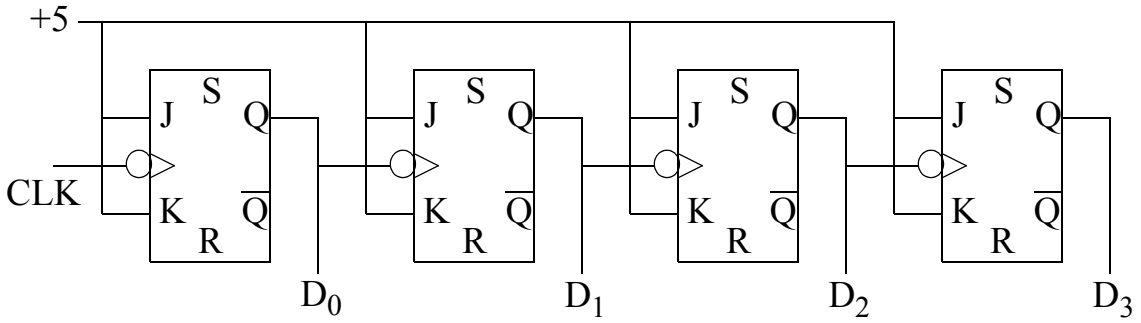
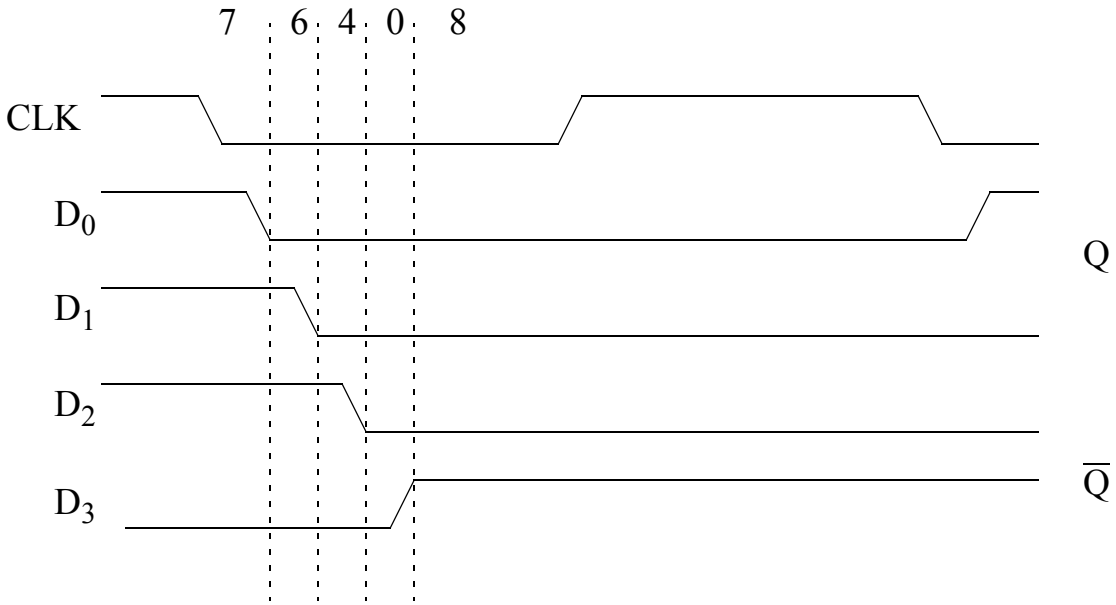
Counters

Ripple Counter

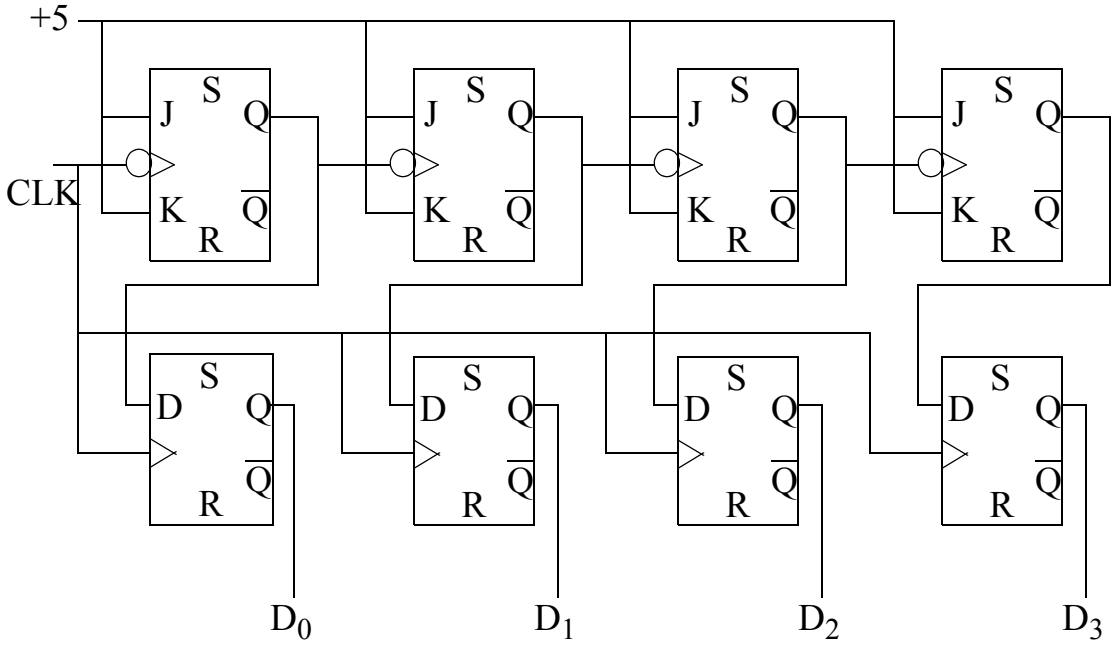




In a ripple counter at a clock edge each data bit much change before the next higher bit can change. The apparent counts that exist during the clock transition are called *transients*.

D-Latch Outputs

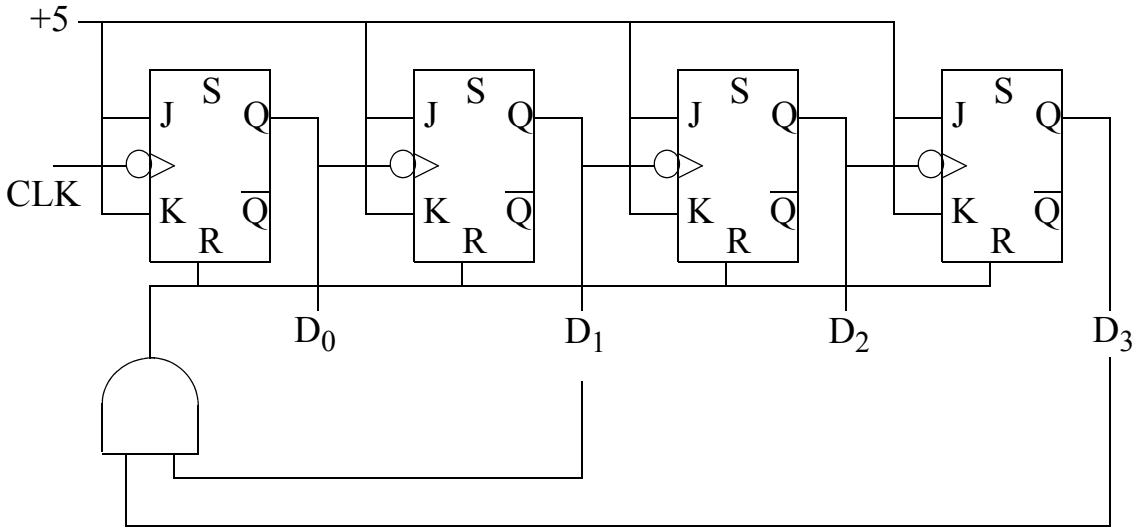
- Clock synchronizes output



- The ripple counter is updated on the falling edge of the clock.
- The D flip-flops are clocked on the rising edge of the clock, long after the values of all bits are set.
- Transients are suppressed.

Arbitrary Counter

Count to 10



- When the clock causes both D_3 and D_1 to be high, a clear is sent to all flip-flops.
- The first case of this count is at the clock from 9 to 10.

Load and Clear Inputs

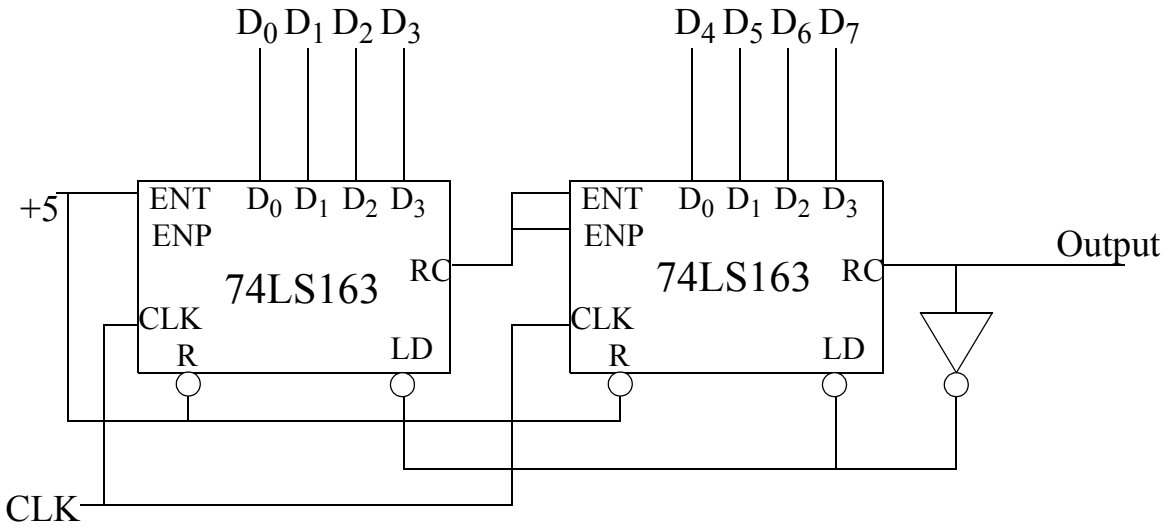
The set and clear of the flip-flops are used in circuits to preload a starting count.

Latched Outputs

Transient problems can be fixed with output latches.

Pulse Generator

- Circuit



- Each chip has four internal flip-flops.
- ENT and ENP are the JK inputs for the flip-flops.
- $\overline{\text{LD}}$ is the $\overline{\text{SET}}$ input for the flip-flops.

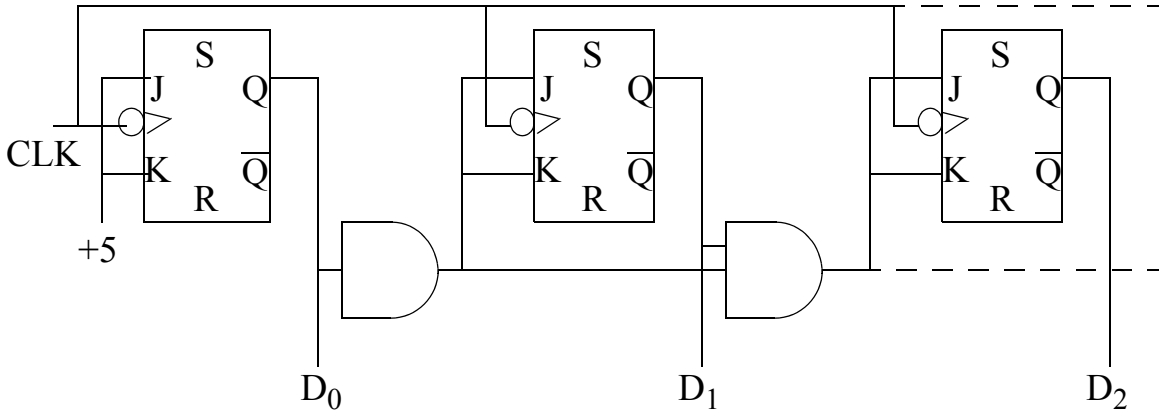
The counter is loaded with a value *x* from 0-255 (0-FF_H). With each clock rising edge the count increases by one. When FF_H is reached, RC goes high. This reloads the counter to repeat the cycle. The output is high for one clock cycle and low for 256-*x* cycles.

Synchronous Counters

Clock all flip-flops at the same time.

1. Reduce propagation time
2. Eliminate transient counts

Divide by 2^n (JK)



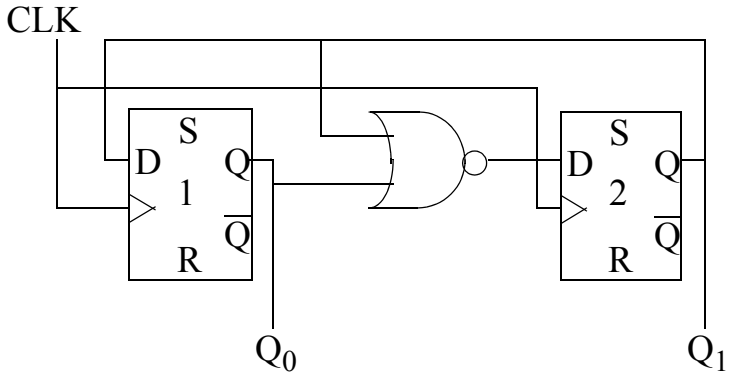
D_0 is dividing the input clock by 2.

D_1 is dividing the input clock by 4. It toggles when $D_0 = 1$.

D_2 is dividing the input clock by 8. It toggles when $D_1 \& D_0 = 1$.

Divide By n

- Divide by 3 (D-type)



- Divide by 3 Truth Table

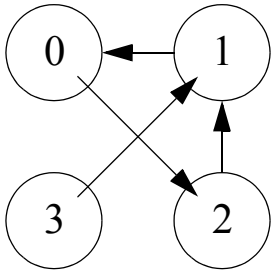
CLK	D_0	Q_0	D_1	Q_1	Count
	0	0	1	0	0
0->1	1	0	0	1	2
0->1	0	1	0	0	1
0->1	0	0	1	0	0
0->1	1	0	0	1	2

State Diagram

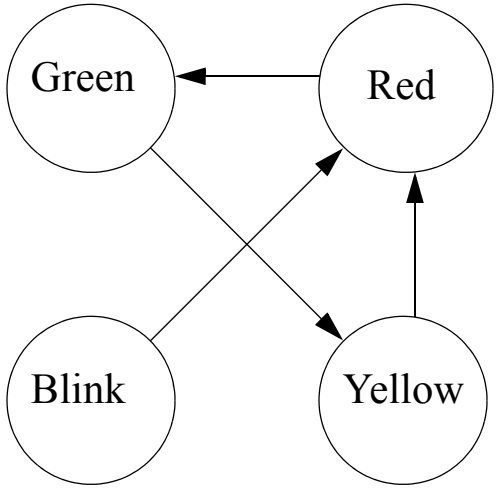
Forbidden States

In the Divide by 3 circuit, $Q_0 = 1$ and $Q_1 = 1$ cannot be reached

If it occurs, $D_0 = 1$ and $D_1 = 0$ so the next count is 1.



- State diagram for traffic signals



Registers

Latches and Registers

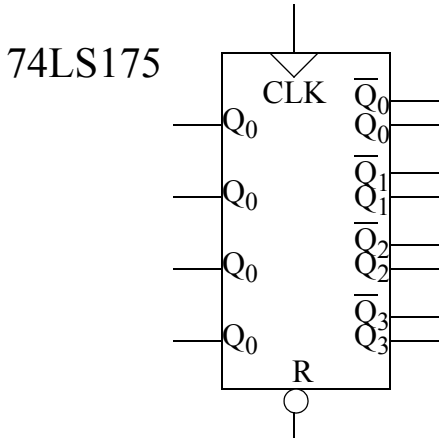
- Multiple flip-flops on one IC with one clock and clear
- One output (or output pair Q/$\overline{Q}$) per input
- Designed to "hold" a set of bits

Transparent Latches

Based on RS flip-flops, these devices pass the input to the output when enabled and hold the output constant when disabled.

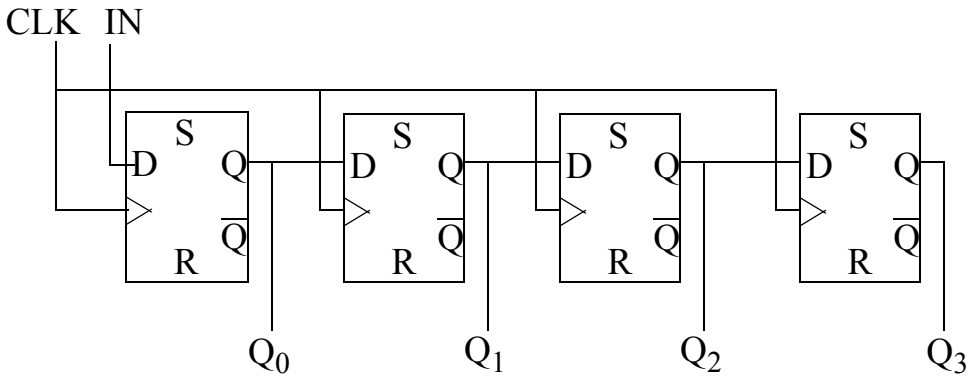
Type D Registers

Based on D-type flip-flops, these devices transfer the input to the output only on a specified clock edge and then only when enabled. Otherwise the output is held constant.



Shift Registers

- Serial In/Parallel Out (SIPO)

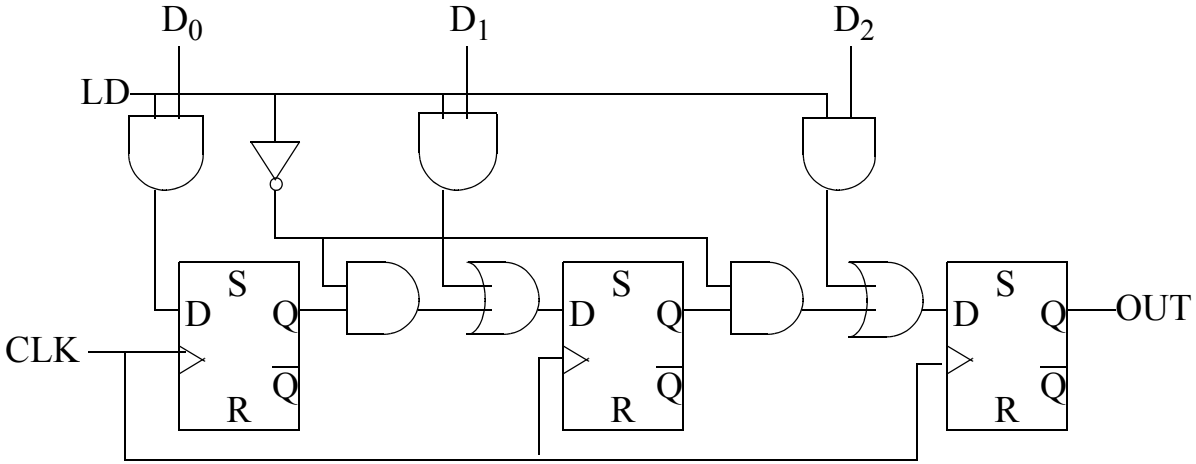


- SIPO Truth Table - bits shift with each clock cycle

CLK	IN	Q_0	Q_1	Q_2	Q_3
	0	0	0	0	0
0->1	1	1	0	0	0
0->1	1	1	1	0	0
0->1	0	0	1	1	0
0->1	0	0	0	1	1
0->1	0	0	0	0	1

Parallel Load

- Parallel In/Single Out (PISO)

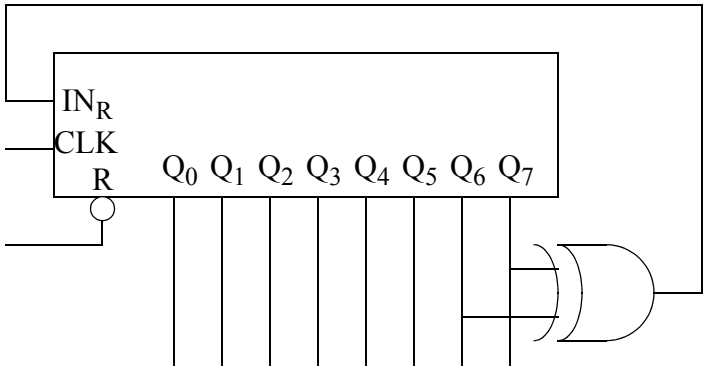


- PISO Truth Table (Data is 0110); LD is parallel load of input data

CLK	LD	Q_0	Q_1	Q_2	Q_3	OUT
0->1	1	0	1	1	0	0
0->1	0	0	0	1	1	1
0->1	0	0	0	0	1	1
0->1	0	0	0	0	0	0
0->1	0	0	0	0	0	0

Shift Register Signal Generators

- Pseudorandom Noise Generator



If the register begins at 0, the input continues to be 0 and there is no change of state.
If the register begins at 1, that one bit will shift through the register at each clock cycle.
When it reaches Q_6 and Q_7 then those two clocks will input a 1 instead of a 0 to the input.
Those two consecutive bits clock through and at the end generate a 101 pattern to the input.
Only after 255 clock cycles does the number 1 reemerge.

The register generates all values from 1-255 in an arbitrary order that is set by the specific feedback through the XOR gate.

Truth Table with Feedback

CLK	$Q_0=Q_2@Q_3$	Q_1	Q_2	Q_3	Count
0->1	1	0	0	0	1
0->1	0	1	0	0	2
0->1	0	0	1	0	4
0->1	1	0	0	1	9
0->1	1	1	0	0	3
0->1	0	1	1	0	6
0->1	1	0	1	1	13
0->1	0	1	0	1	10
0->1	1	0	1	0	5
0->1	1	1	0	1	11
0->1	1	1	1	0	7
0->1	1	1	1	1	15
0->1	0	1	1	1	14
0->1	0	0	1	1	12
0->1	0	0	0	1	8

Feedback Changes

- Feedback $Q_1@Q_3$

CLK	$Q_0=Q_1@Q_3$	Q_1	Q_2	Q_3	Count
0->1	1	0	0	0	1
0->1	0	1	0	0	2
0->1	1	0	1	0	5
0->1	0	1	0	1	10
0->1	0	0	1	0	4
0->1	0	0	0	1	8
0->1	1	0	0	0	1

This feedback combination does not go through all 15 possible combinations, but only 7.

There are 6 possible feedback choices for 4 bits:

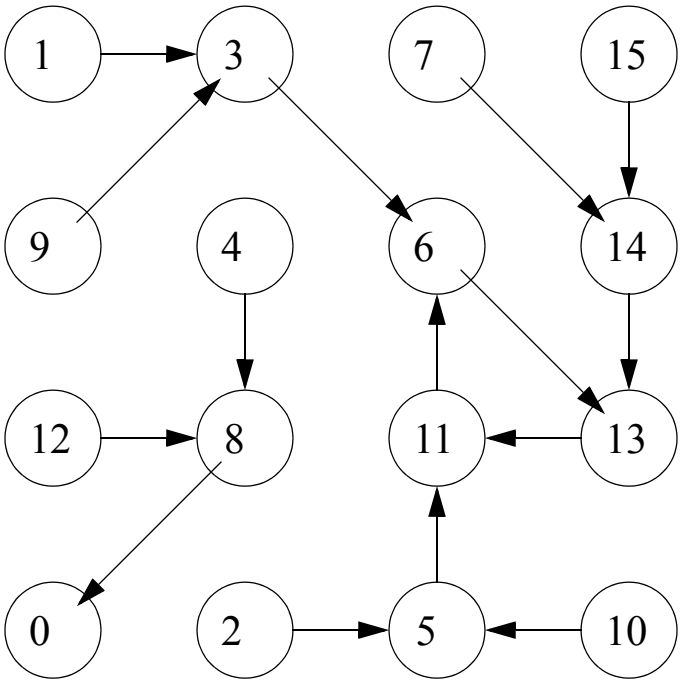
$Q_0 = Q_2@Q_3$ gives 15 numbers; $Q_0 = Q_1@Q_3$ gives 7 numbers

$Q_0 = Q_0@Q_3$ gives 15 numbers; $Q_0 = Q_1@Q_2$ gives 7 numbers after 2 is reached

$Q_0 = Q_0@Q_2$ gives 7 numbers after 3 is reached; $Q_0 = Q_0@Q_1$ gives 3 numbers after 6 is reached

Pseudorandom State Diagram

- Feedback $Q_1@Q_3$



$Q_0 = Q_1@Q_3$