

Sequential Logic



A *gate* is a circuit element that operates on a binary signal.

Combinatoric logic uses Boolean algebra to calculate the output from the input.

Sequential logic requires knowledge of the previous state of the circuit.

Logic Operations - Sequential Logic

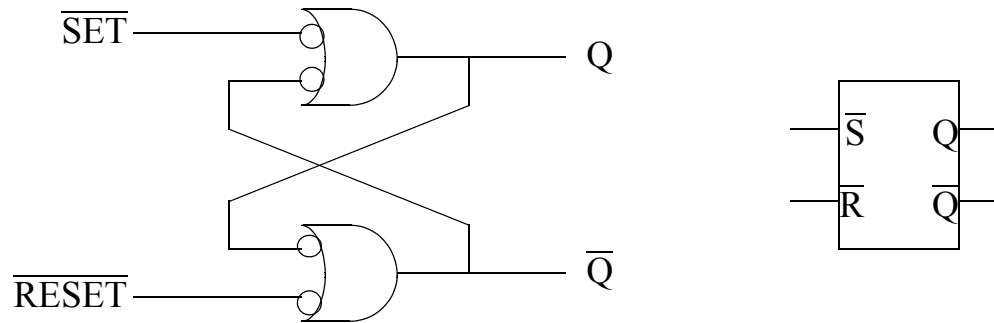
Sequential devices typically have three (four) methods of description:

1. Truth table
2. Circuit symbol (gate equivalent)
3. Timing diagram

RS (Set-Reset) Flip-Flop

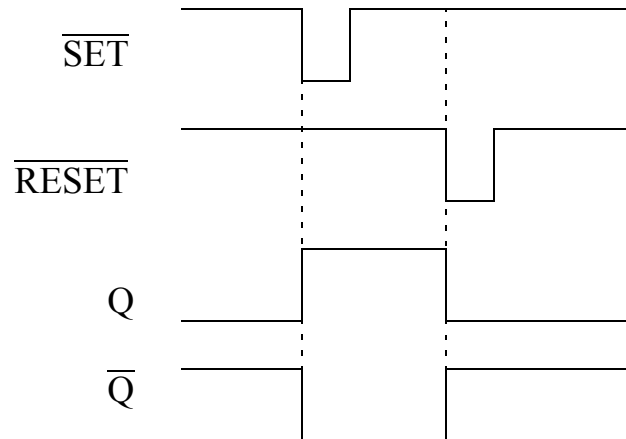


- RS Flip-flop Diagram



Able to be forced into one state or another with input to SET or RESET.

- RS Flip-flop Timing

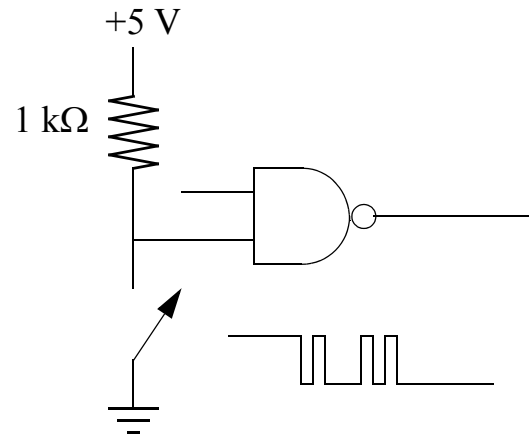


SET and RESET cannot be used simultaneously - ambiguous result.

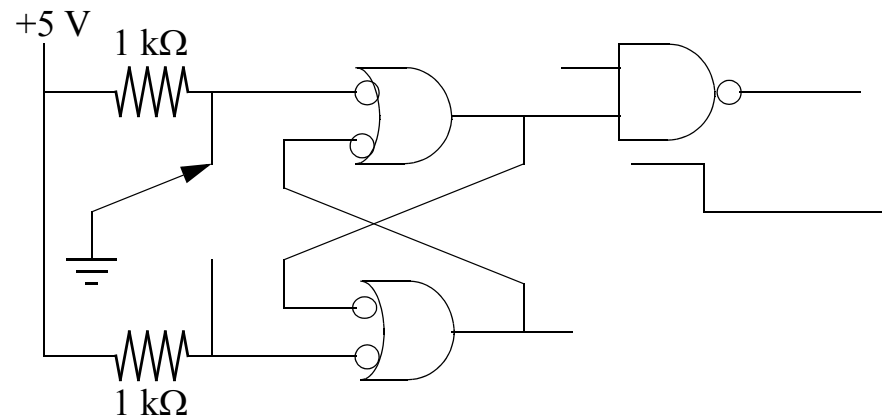
Switch Debouncer



- Normal Switch



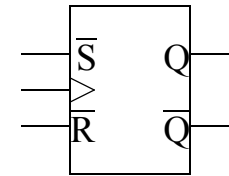
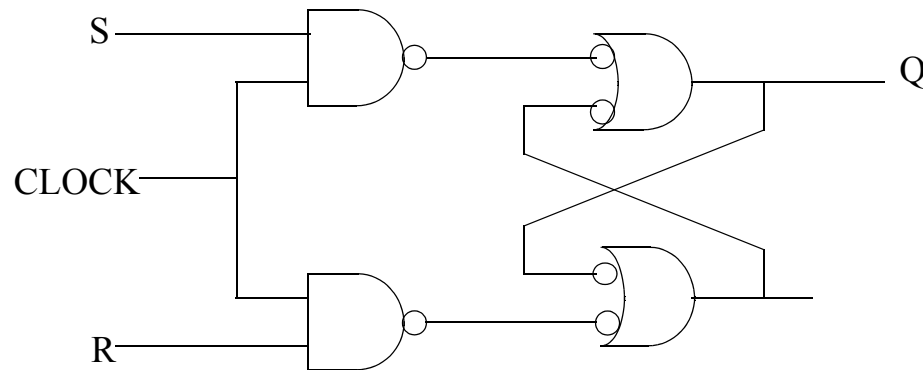
- Debounced Switch



Triggered Flip-Flops



- Clocked RS Flip-flop



The extra NAND gates allow the CLOCK to control whether S and R make it to the flip-flop.

If CLOCK=0 the inputs to the flip-flop are disabled and Q stays constant.

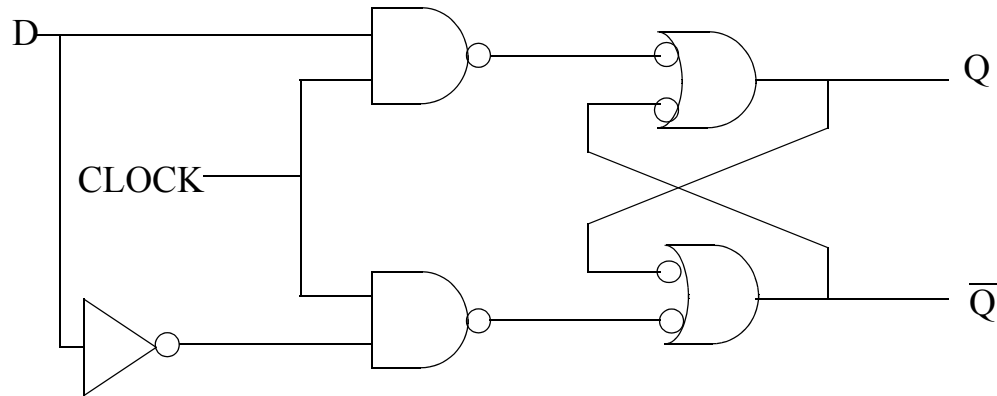
If CLOCK=1 the inputs are active and Q samples S and R.

Disadvantage: If S or R change during the clock pulse, only the final state of the RS flip-flop is preserved when CLOCK=0 again.

D-Type Flip-Flop



- Level-Sensitive Clock



Circuit is identical to a clocked RS flip-flop, except one input is inverted to form the other input.

CLK	D	Q	\bar{Q}
0	0	Q	\bar{Q}
0	1	Q	\bar{Q}
1	0	0	1
1	1	1	0

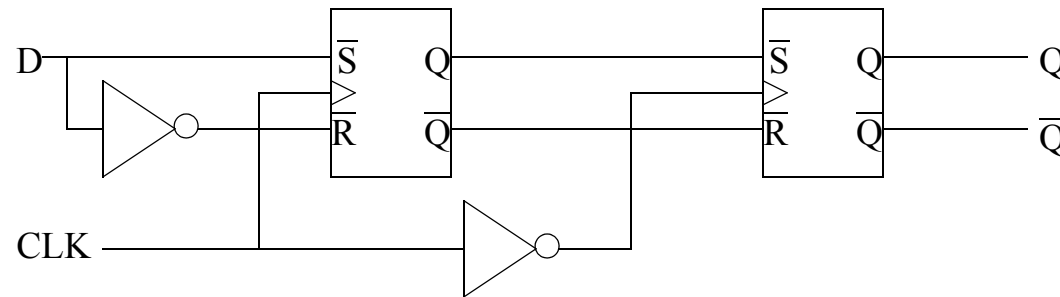
With only one input the indeterminate state ($R=S=1$) is avoided.

D can make many transitions while $CLK = 1$, only the last level is stored when $CLK = 0$.

Edge-Triggered Flip-Flops



- Master-Slave Flip-Flop



This circuit consists of two level-sensitive D-type flip-flops.

During CLK=1, the first flip-flop is enabled, but the second is disabled (memory only).

During CLK=0, the first flip-flop is disabled, but the second is enabled, so it samples what ever is held at that time on flip-flop 1.

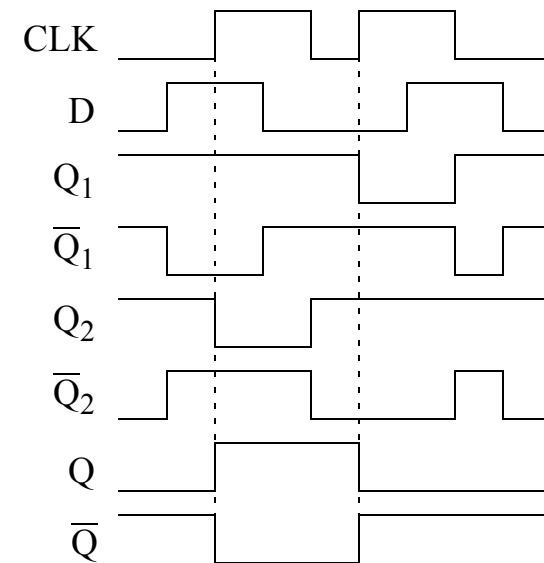
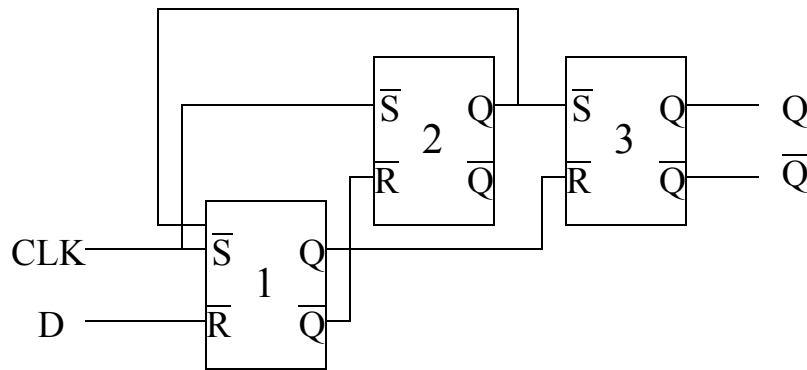
The output Q can only change exactly as CLK goes from 1 to 0.

This is a negative edge trigger.

Positive Edge Trigger



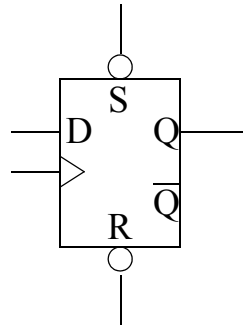
- Three RS flip-flops



Set and Clear Inputs



- Most edge-triggered flip-flops come with both set and clear options that work like S and R from an RS flip-flop.



If SET=0, then Q is forced to 1, and \bar{Q} to 0.

If CLEAR=0 (RESET), then \bar{Q} is forced to 1, and Q to 0.

SET and CLEAR take effect regardless of the state of CLK.

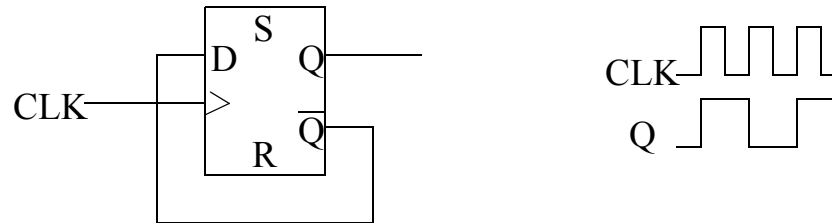
- D-type flip-flops also come with positive logic SET and CLEAR.

Divider



Dividers - Divide by 2

- D-type Flip-Flop



D is always set with \overline{Q} , so at each rising edge Q switches.

There is no confusion at the rising edge since there is a 10ns propagation delay through the flip-flop (74HC74), and the output needs to be stable for only 3 ns.

JK Flip-Flops

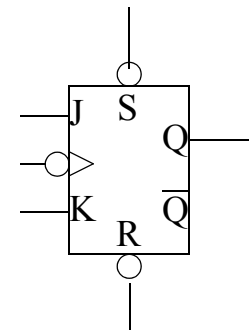
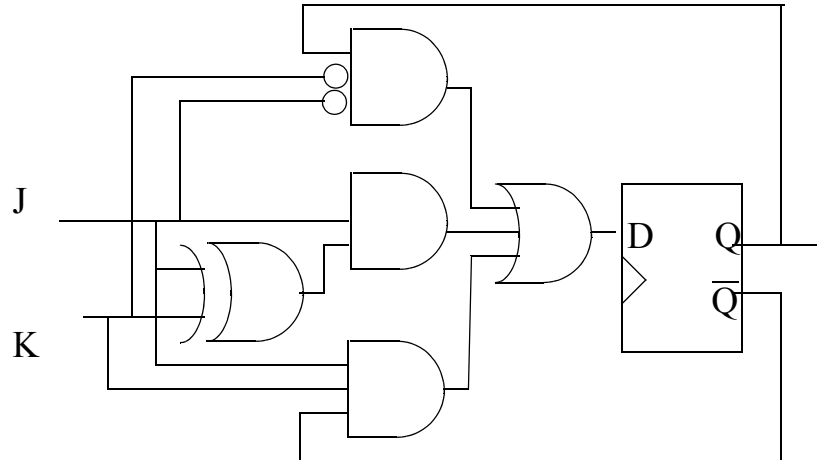


- Logic

2-Input clocked flip-flop, like D-type with the following input:

$$D = (J \oplus K) \cdot J + J \cdot K \cdot \bar{Q} + \bar{J} \cdot \bar{K} \cdot Q$$

- Circuit (may include set and clear)



- J and K different, $Q = J$
- $J = K = 1$, $Q = \text{not } Q$
- $J = K = 0$, Q holds

JK Divider



- JK Flip-Flop

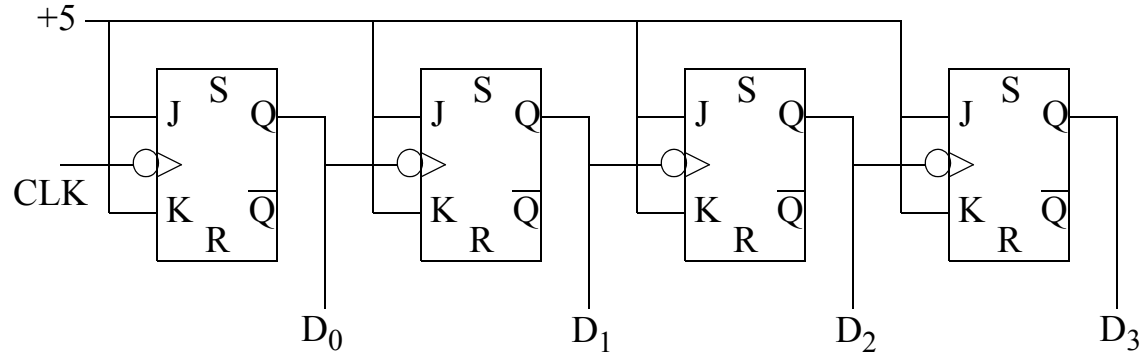


Holding both inputs of a JK high causes a toggle.

Multi-Stage Divider



- Divide by 2^n



Each JK flip-flop is set to divide the clock by 2.

D₀ is dividing the input clock by 2.

D₁ is dividing the input clock by 4.

D₂ is dividing the input clock by 8.

D₃ is dividing the input clock by 16.

This can be extended to any arbitrary length.

Divider Truth Table



- Divide by 16 Truth Table

CLK	D ₀	D ₁	D ₂	D ₃	Count
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	1
1	1	0	0	0	1
0	0	1	0	0	2
1	0	1	0	0	2
0	1	1	0	0	3
...
1	0	1	1	1	14
0	1	1	1	1	15
1	1	1	1	1	15
0	0	0	0	0	0