Logic Gates

A *gate* is a circuit element that operates on a binary signal.

Logic Operations - Boolean Algebra

Logic operations typically have three methods of description:

1. Equation symbol

   Typically a mathematical symbol operating on variables, such as

   $A \qquad \overline{A} \qquad A + B \qquad A \bullet B \qquad A \oplus B$

2. Truth table

   Lists all possible inputs, followed by the expected output

3. Circuit symbol

Boolean Logic

- Group Properties

$$A \bullet B = B \bullet A$$

$$A + B = B + A$$

$$A \bullet (B + C) = (A \bullet B) + (A \bullet C)$$

- DeMorgan's Theorem

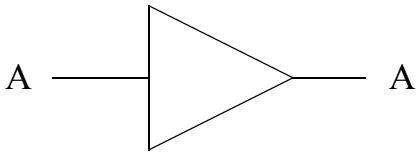
$$\overline{A \bullet B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \bullet \overline{B}$$

- Unary operations act on a single input.
- Binary operations act on two inputs to produce one output.

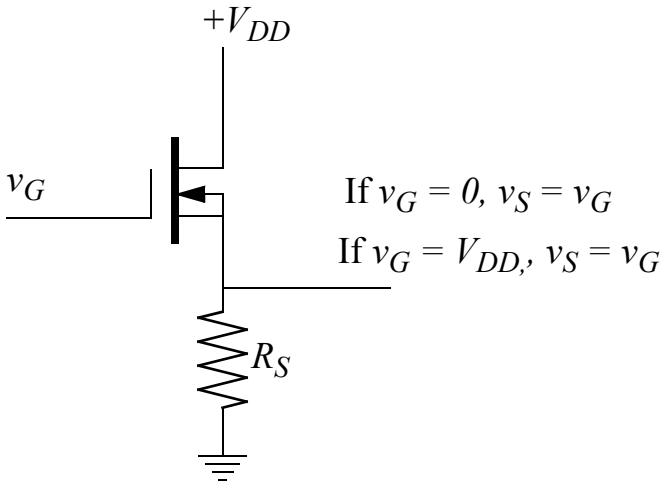
Identity

- Identity gate



A_{in}	A_{out}
0	0
1	1

- Electronic identity

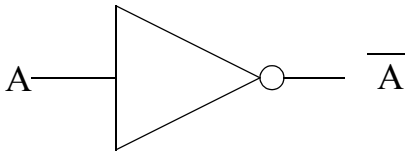


Source Follower Buffer

- Buffers have no effect on the logic value in a circuit.

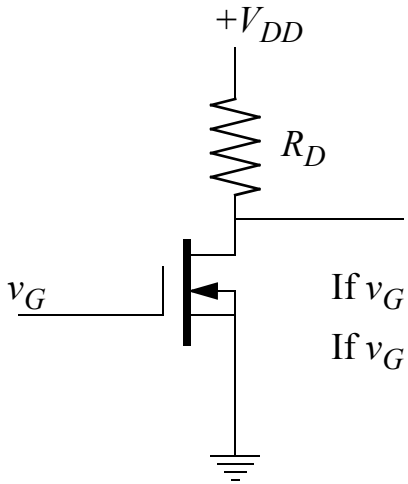
Inverse

- Inverse



A_{in}	$\overline{A}_{out}$
0	1
1	0

- Electronic Inverse



If $v_G = 0$, $v_D = V_{DD} - v_G = V_{DD}$

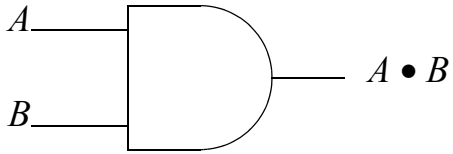
If $v_G = V_{DD}$, $v_D = V_{DD} - v_G = 0$

Common Source Inverter

- Inverters change a signal from one of two states into the other.
- A circle at the input represents an inverted input.

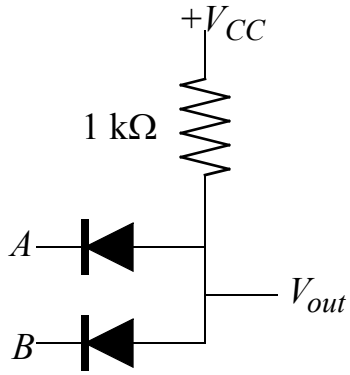
Logical AND

- AND gate



A_{in}	B_{in}	$A \bullet B_{out}$
0	0	0
0	1	0
1	0	0
1	1	1

- Electronic AND

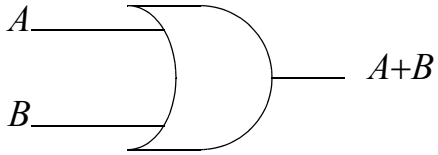


For V_{out} to be at $+V_{CC}$ both A and B must be within 0.6 V of $+V_{CC}$.

- Disadvantages of this circuit are that a low output is 0.6 V, the output load will be seen by the signal, and the circuit is slow to respond due to the resistor pull-up.

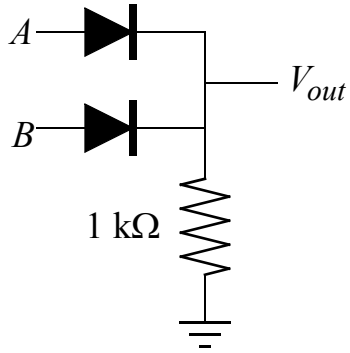
Logical OR

- OR gate



A_{in}	B_{in}	$A+B_{out}$
0	0	0
0	1	1
1	0	1
1	1	1

- Electronic OR

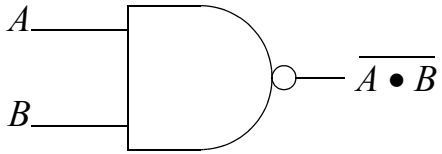


For V_{out} to not be 0 V either A or B must be over 0.6 V.

- Disadvantages of this circuit are that a high output is 0.6 V below the input, the output load will be seen by the signal, and the circuit is slow to respond due to the resistor pull-down.

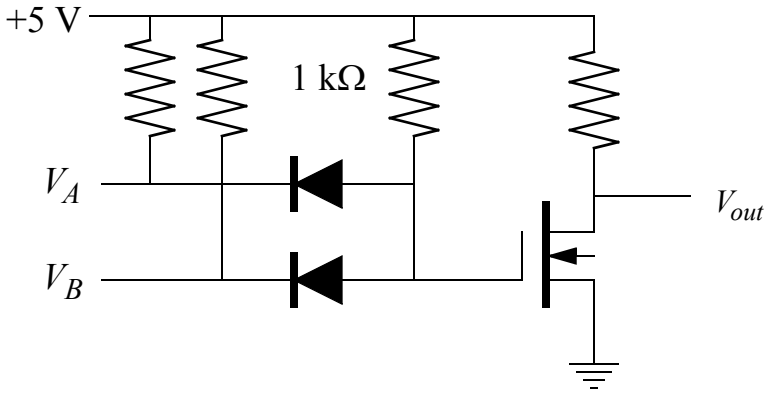
Not-AND

- NAND gate



A_{in}	B_{in}	$\overline{A \bullet B}_{out}$
0	0	1
0	1	1
1	0	1
1	1	0

- Electronic NAND



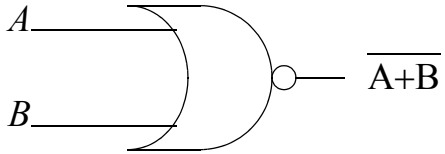
- NAND gates can be used to create other logic gates.

$$\overline{(\overline{A \bullet B}) \bullet (\overline{A \bullet B})} = \overline{(\overline{A \bullet B})} = A \bullet B$$

$$\overline{(\overline{A \bullet A}) \bullet (\overline{B \bullet B})} = \overline{\overline{A} \bullet \overline{B}} = A + B$$

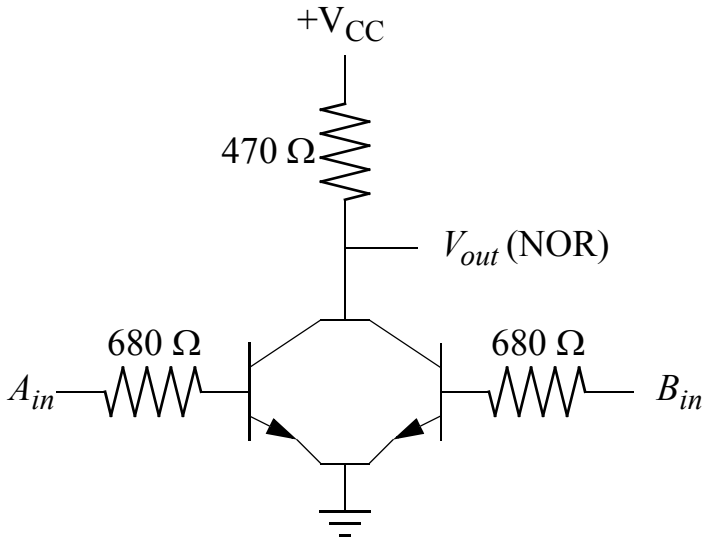
Not-OR

- NOR gate



A_{in}	B_{in}	$\overline{A+B}_{out}$
0	0	1
0	1	0
1	0	0
1	1	0

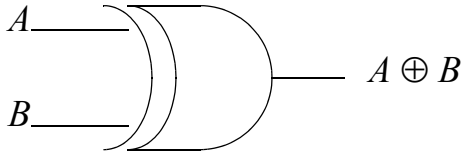
- Electronic NOR (Resistor-Transistor Logic)



- Like NAND, other gates can be made from NOR gates.

Exclusive OR

- XOR gate



A_{in}	B_{in}	$(A \oplus B)_{out}$
0	0	0
0	1	1
1	0	1
1	1	0

- The exclusive OR is true if the inputs are different.
- There are a number of equivalent logical constructions for XOR:

$$A \oplus B = (A + B) \bullet \overline{(A \bullet B)}$$

$$A \oplus B = \overline{(\bar{A} \bullet \bar{B})} \bullet \overline{(A \bullet B)}$$

$$A \oplus B = \overline{(\bar{A} \bullet \bar{B}) + (A \bullet B)}$$

$$A \oplus B = (A \bullet \bar{B}) + (\bar{A} \bullet B)$$

$$A \oplus B = \overline{\overline{(A \bullet \bar{B})} \bullet \overline{(\bar{A} \bullet B)}}$$

Logic Levels

Boolean Levels

Logic levels are *T*=True and *F*=False.

Alternate levels are 1=True and 0=False.

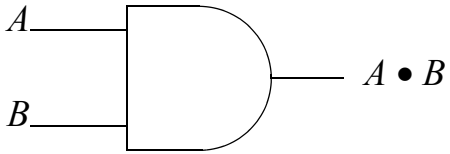
Electronic Levels

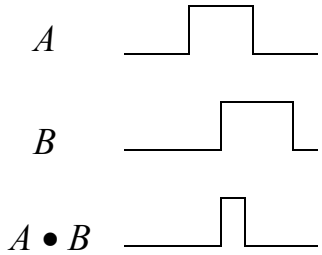
Logic levels are *H*=High and *L*=Low.

Alternate levels are 1=High and 0=Low.

Positive Logic

- High = TRUE



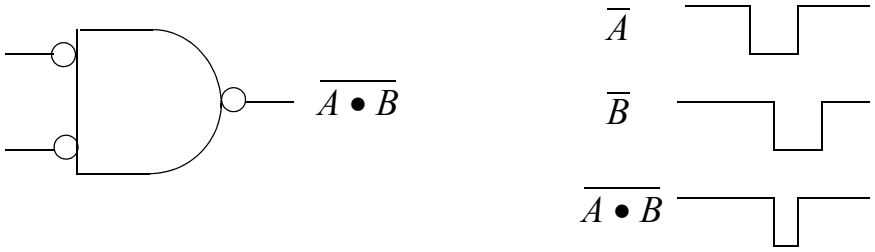


Timing diagram

- High inputs correspond to logical TRUE.

Negative Logic

- High = FALSE



- High inputs correspond to logical FALSE.
- A negative logic NAND is equal to a positive logic OR gate.
- By DeMorgan's Theorem:

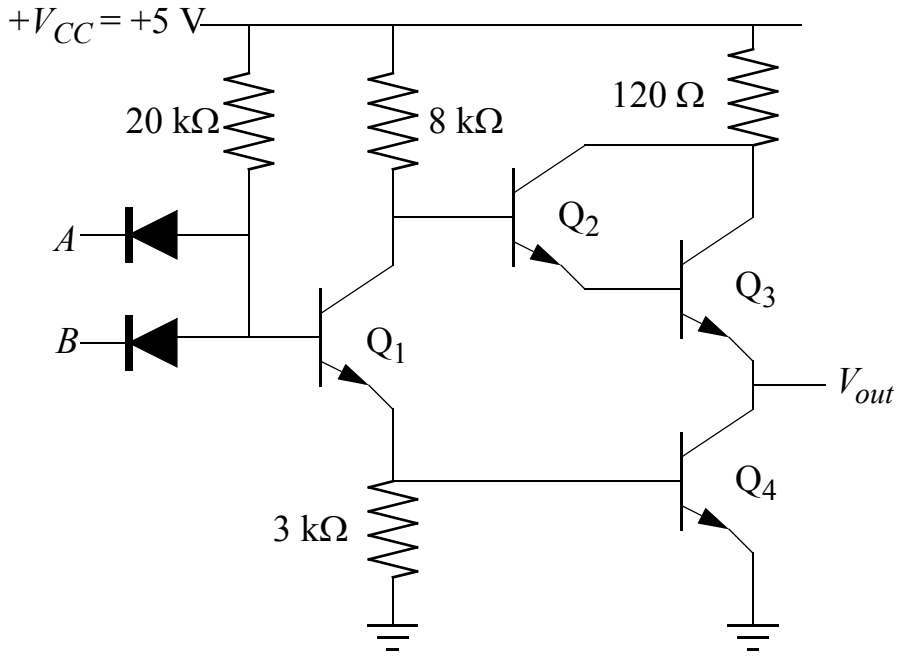
$$\overline{\overline{A} \bullet \overline{B}} = A + B$$

Note: There can be confusion since in negative logic a logical "1" is not an electrical "1".

- Negative logic frequently appears in systems where the usual operating point should be HIGH. For example, logic gates may use less current if operated at HIGH.

TTL - Transistor-Transistor Logic

- NAND - 74LS00



The diodes and 20 kΩ resistor make a simple AND-gate.

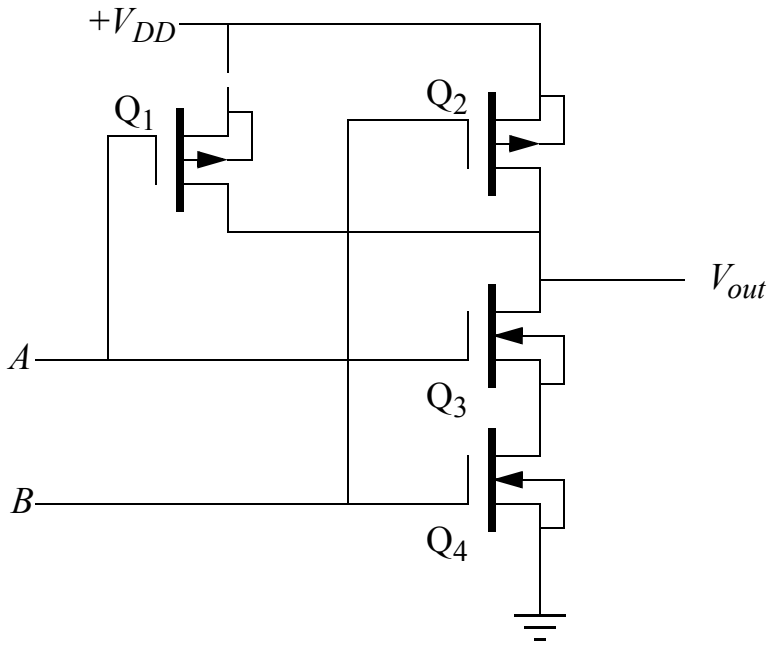
The transistor at Q_1 forms an inverter to the base of Q_2 and Q_4.

The transistors Q_2, Q_3, and Q_4 form a "push-pull" amplifier.

- If *A* and *B* are HIGH, the base of Q_1 is at 5 V, and Q_1 is on. That puts the bases of Q_2 and Q_4 at about 1.4 V turning both on. V_{out} is then pulled to ground plus a C-E drop of 0.1 to 0.2 V.
- If *A* or *B* is LOW, the base of Q_1 is at 0.6 V and is off. This holds the base of Q_2 at 5 V and Q_4 at ground. Q_3 is on and V_{out} is at 4.4 V. due to a diode drop across the Darlington Q_2Q_3.

CMOS Logic

- NAND 4011B



The CMOS MOSFETs are connected as switches.

HIGH at A and B turn on Q_3 and Q_4 while turning off Q_1 and Q_2.

LOW at A and B turn on Q_1 and Q_2 while turning off Q_3 and Q_4.

- If both Q_3 and Q_4 are on then V_{out} is at ground, otherwise either Q_1 or Q_2 will be on pulling V_{out} up to V_{DD}.