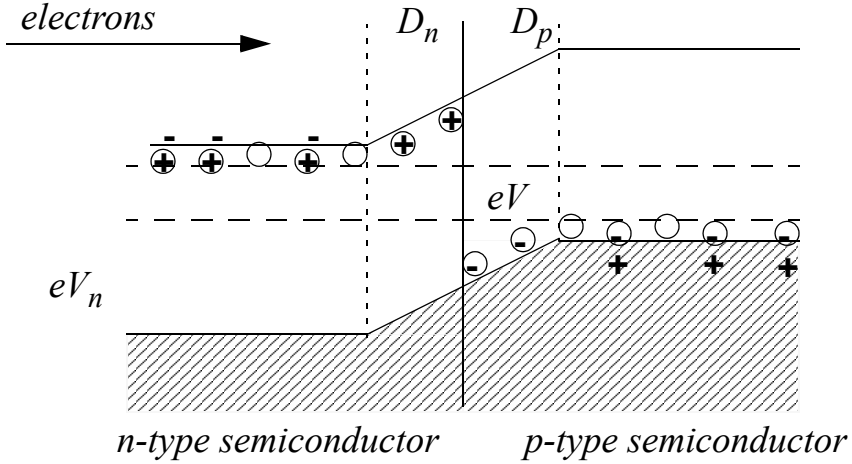
Field Effect Transistors

Electric Fields at a Junction

- Forward-biased p-n junction



- The field and potential in the semiconductor is

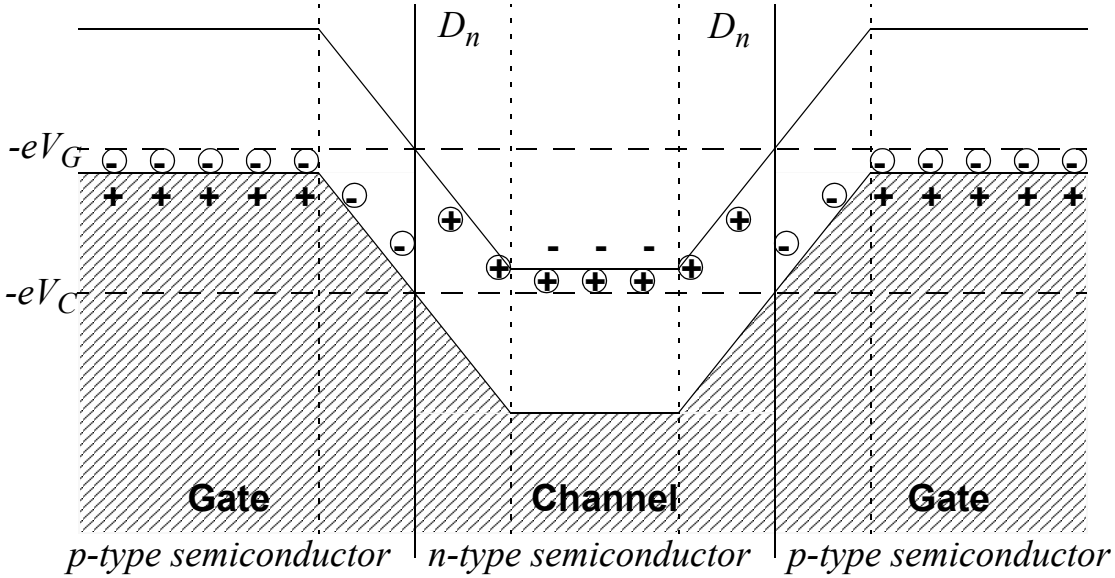
$$E = \frac{Nex}{\varepsilon_r \varepsilon_0} \qquad V = \frac{Nex^2}{2\varepsilon_r \varepsilon_0}$$

- The depth of depletion in the semiconductor is

$$D_n = \sqrt{\frac{2\varepsilon_r \varepsilon_0 (V_n + V)}{N_n e}} \qquad D_p = \sqrt{\frac{2\varepsilon_r \varepsilon_0 (V_p + V)}{N_p e}}$$

p-n Junction Sandwich

- An n-type semiconductor sandwiched in a p-type material, with reverse bias



- The depth of the depletion is

$$D_n = \sqrt{\frac{2\varepsilon_r\varepsilon_0(V_{GC}+V_0)}{N_n e}}$$

- The resistance R in the channel is based on the resistivity ρ, length L and cross sectional area A:

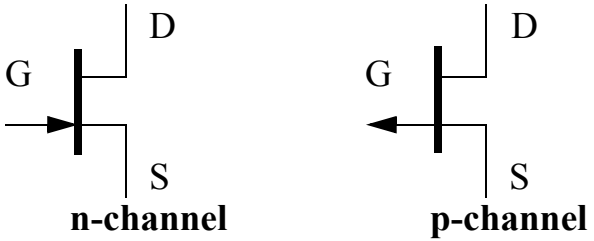
$$R = \rho L/A$$

- When the area is reduced by increasing the voltage, the resistance increases

$$R = R(V_{GC})$$

Junction Field Effect Transistor

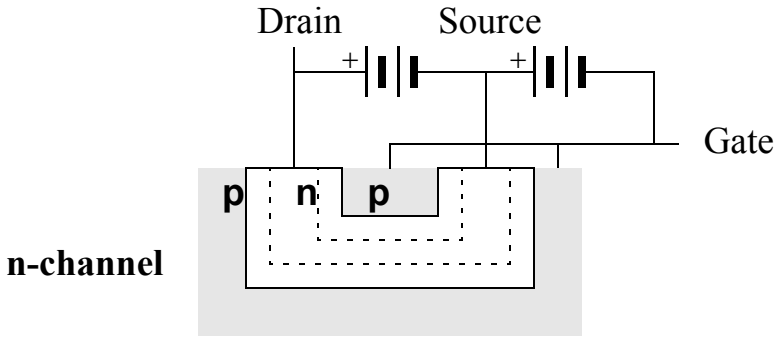
- JFET schematic symbol:

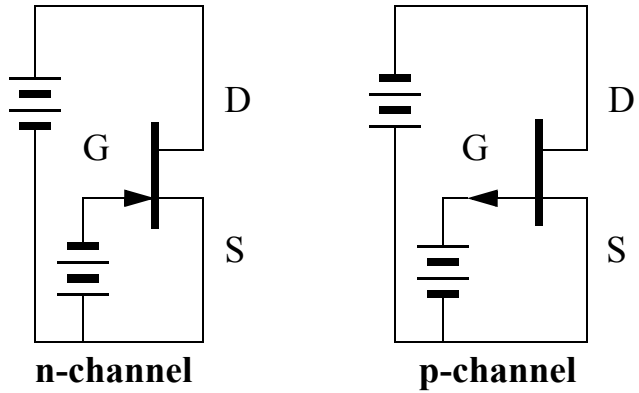


- The channel in a field effect transistor has a finite length and a measurable resistance, and it can be treated like a resistor in a circuit.
- The drain and source are connected to two ends of the channel.
- The gate forms a diode with the channel.
- The gate impedance is a reverse-biased diode so it is large: $> 10^{9}\ \Omega$.

JFET Connections

- The *bias* on the gate creates a variable resistor in the channel.





- The voltage between the gate and source controls the channel.
- The voltage between the source and drain creates the current through the channel

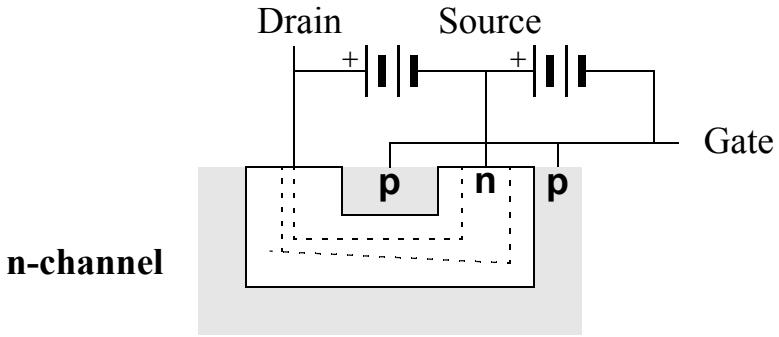
$$I_D = V_{DS} / R(V_{GS})$$

Field Effect Pinch Off

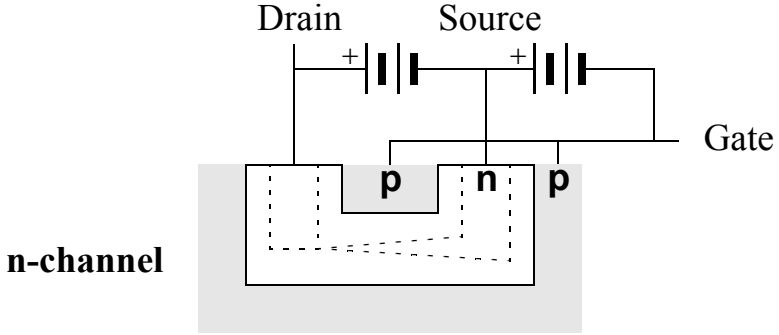
- For larger V_{DS} the channel is narrower at the drain than at the gate.

$$D_S \propto \sqrt{V_{GS} + V_0}$$

$$D_D \propto \sqrt{V_{DS} + V_{GS} + V_0}$$



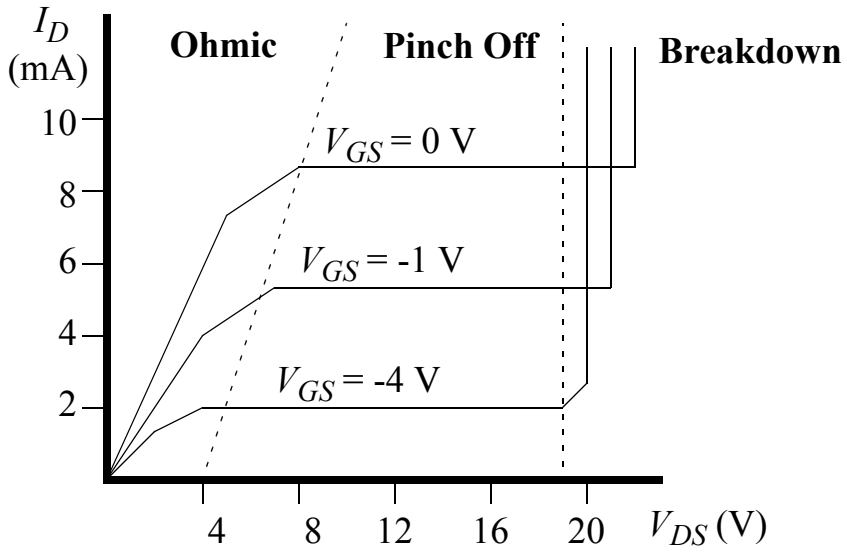
- Eventually the channel is restricted to give a constant current I_D.



- This is called field effect *pinch-off*. If too large, the reverse-bias diode breaks down.

JFET Voltage - Current Curves

- Curves are for specific V_{GS} and compare I_D to V_{DS}.



- V_{GS} is reversed bias so $V_{GS} < 0$.
- In the ohmic region:

$$1/R_{DS} = I_D/V_{DS} = 2k[(V_{GS} - V_{TR}) - V_{DS}/2]$$

$$I_D = 2kV_{DS}[(V_{GS} - V_{TR}) - V_{DS}/2]$$

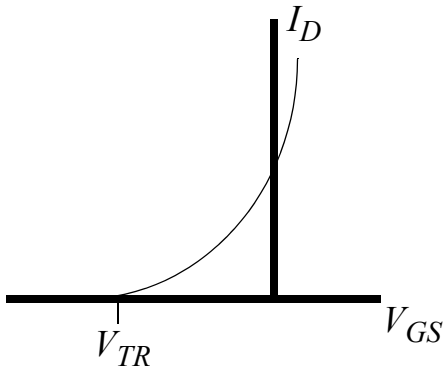
V_{TR} is the threshold voltage for operation

k depends on the FET, varies with temperature ($T^{-3/2}$)

Transconductance

- In the pinch-off (saturation) region:

$$I_D = k(V_{GS} - V_{TR})^2$$



- The slope of the curve I_D vs. V_{GS} at constant V_{DS} is defined as g_m.

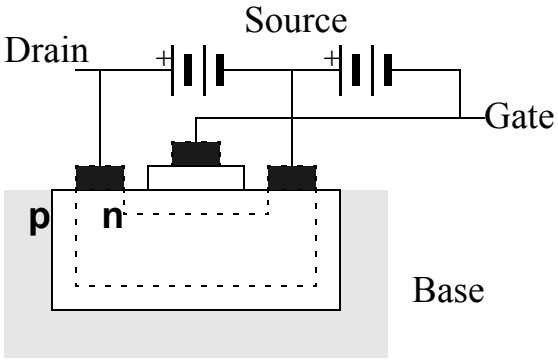
- The transconductance: $g_m = \left(\frac{\partial i_D}{\partial v_{GS}}\right)_{V_{DS}}$

  This is typically 1-30 mS.

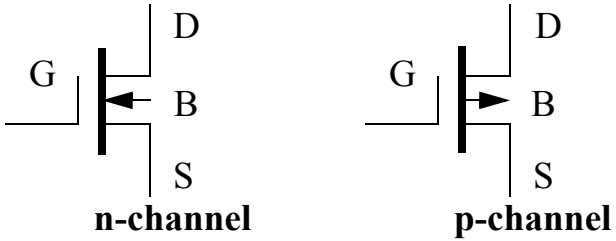
MOSFET

Metal-Oxide-Semiconductor FET

- Depletion n-channel MOSFET

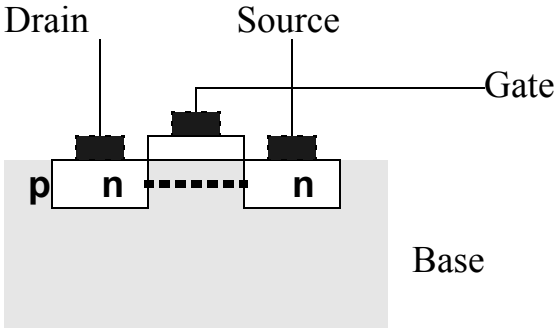


- The metal contact at the gate is separated by an insulating layer
- Very high input impedance ($10^{14}\ \Omega$)
- With no gate - low resistance from source to drain, negative gate the resistance increases
- Base bias affects channel width, used to set operating point for gate
- Schematic symbol:

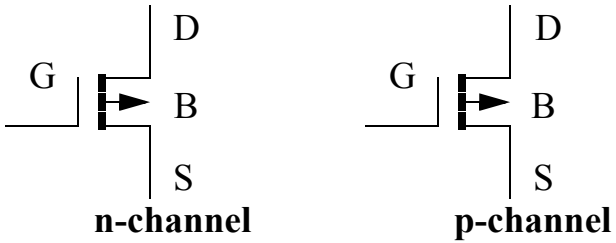


Enhancement MOSFET

- Enhancement n-channel MOSFET



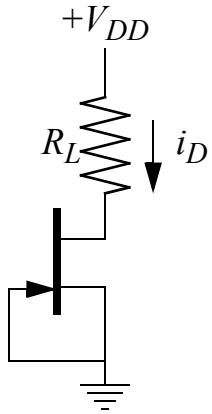
- Depending on the sign of V_{DS} either source-base or drain-base is reverse biased.
- The source and drain are heavily doped to prevent field penetration into the n-type material.
- Positive voltage on the gate induces a field into the base. When the p-type conduction band is lowered to the n-type band current flows into the p-type material and a channel is formed.
- Schematic symbol:



Current Source

Common Source

- The source and gate are grounded, and the drain has a load.



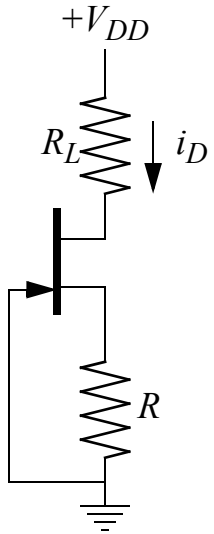
- If $V_{DS} > 2$ V, the FET is in the pinch-off region and delivers a constant current. The limit is $V_{DD} - i_D R_L > 2$ V.

$$I_D = k(V_{GS} - V_T)^2 = k(V_T)^2$$

- These two-terminal devices are sold as current regulators with a range from 0.1 - 10 mA.
- Disadvantages are that they are temperature dependent (0.4% / °C)
- Output current can vary with output voltage.

Bias Resistor

- The gate is grounded, but a resistor biases the source.



- The self-biased FET operates at

$$V_{GS} = i_D R$$

  This is negative, and reduces the FET current from the maximum.
- Current variations are reduced because of the feedback through R.
- With a fixed resistive load this provides a constant voltage.