Physics 375, Laboratory 17
Counters

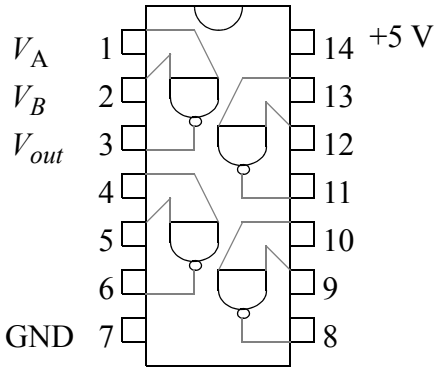
Overview

The purpose of these experiments is to use flip-flops to build counting circuits.

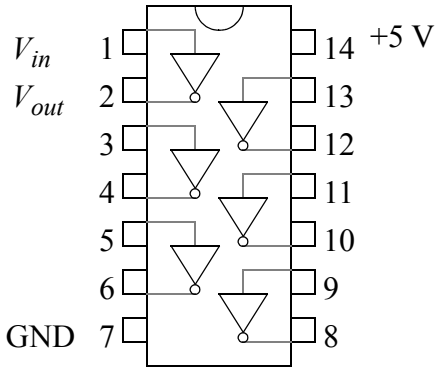
Components

To use any of the gates in these chips, they must be attached to both power (+5 V) and ground.

The 74LS00 is an integrated circuit based on low-power schottky technology that includes 4 NAND gates. The 74HC04 is an integrated circuit based on CMOS technology that includes 6 inverters. The pinouts for the 74LS00 and 74C04 are shown below.

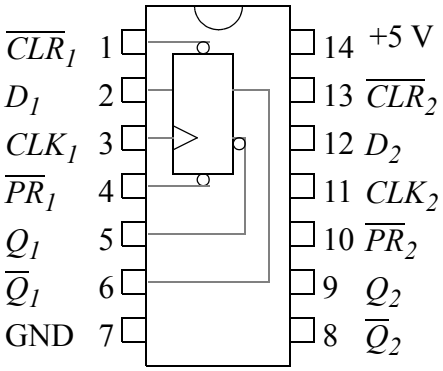


74LS00

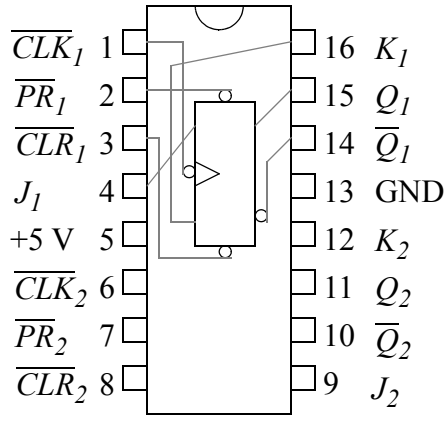


74HC04

The 74LS74 and 74LS76 are integrated circuits with 2 complete flip-flops in each chip. The '74 is a D-type flip-flop with one flip-flop on pins 1-6 and the other flip-flop on pins 8-13. The '76 is a JK-type negative-edge trigger flip-flop with one flip-flop on pins 1-4,14-16 and the other flip-flop on pins 6-12. The pinouts for the 74LS74 and 74LS76 are shown below.



74LS74



74LS76

1. Ripple Counter

Connect 4 D-type flip-flops (74LS74) as toggles with 4 LEDs to form the circuit in Fig. 1. Wire the unused Set and Reset pins to +5 V.

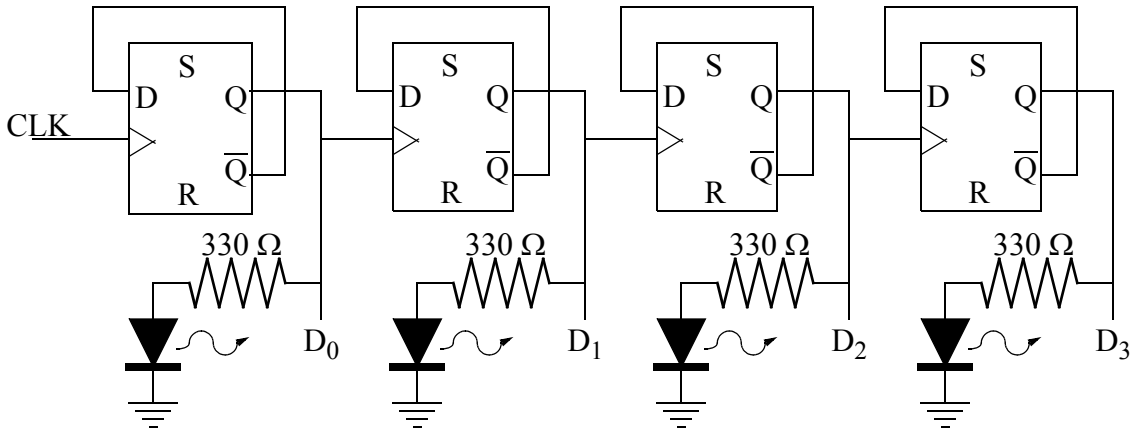


Figure 1: 4-Bit Ripple Counter

Use a TTL square wave at 10 KHz as the input clock. Use the oscilloscope to make a timing diagram of each of the clock and four output bits. Measure the time difference between the input clock edge and the edge of each data bit (trigger the scope on the data bit.) Slow the input clock speed to 1 Hz. Read the LEDs as binary numbers and write the count sequence as a truth table.

2. Synchronous Divide-by-5 Counter

Build a divide-by-5 counter from JK flip-flops (74LS76) as shown in Fig. 2 (Use a NAND and inverter or two NANDs to make the AND-gate, connect all unused JK and set, reset inputs to +5 V). Use a 10 KHz clock and drawn the timing diagram of the outputs. Measure any transients in the output and compare to the ripple counter in part 1. Slow the clock to 1 Hz and use LEDs to confirm the truth table.

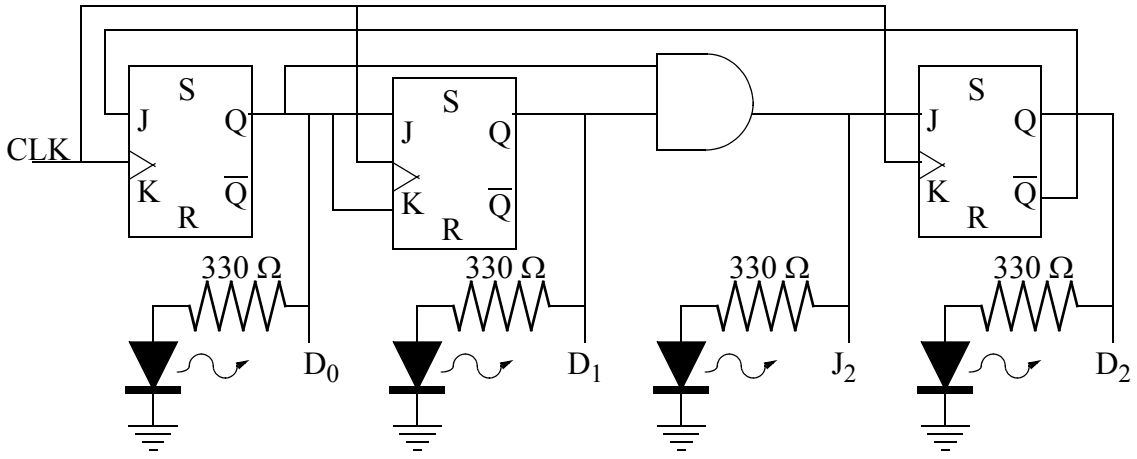


Figure 2: Divide-by-5 Counter