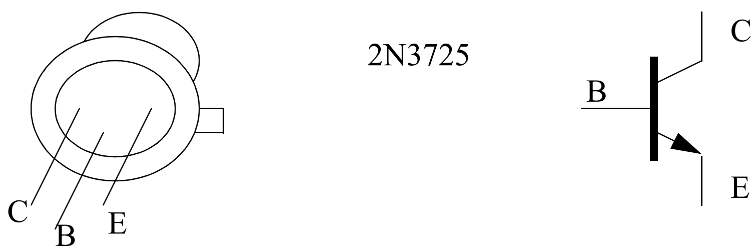
Physics 375, Laboratory 8
Transistor Logic

Overview

The purpose of these experiments is to test the DC properties of JFETs. The properties of transistor switches are also studied.

Background

The 2N3725 is a high-current npn transistor. The 2N3725 comes in a TO-5 metal case with leads for emitter, base and collector.

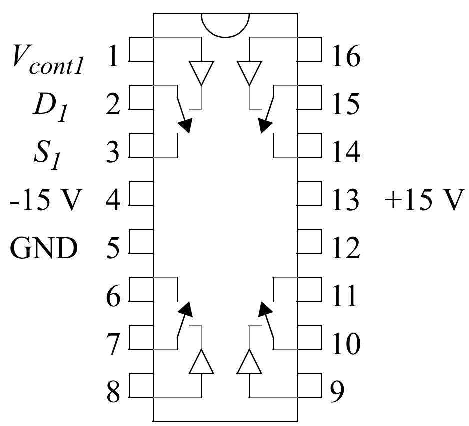


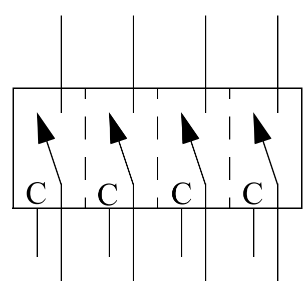
The 2N3725 has maximum ratings as follows:

$V_{CE} < 50$ V, $V_{CB} < 60$ V, $V_{EB} < 6.0$ V

$I_C < 1.5$ A, $P = I_C V_{CE} < 1$ W

The CMOS switch is available in an integrated circuit by Analog Devices called the ADG202A that includes 4 switches. Each switch operates independently, but all use the same power and ground. The pinouts for the ADG202A are shown below.

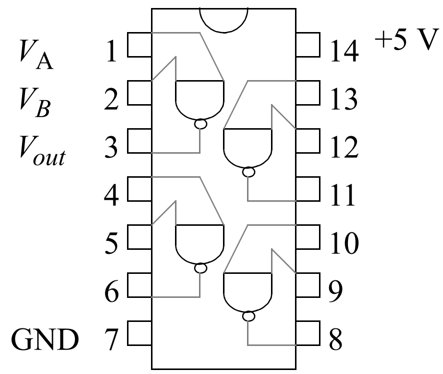




ADG202A

To use any of the gates in the chip, it must be attached to both power (+15 V and -15V) and ground.

Some of the most common TTL logic gates are in the 7400 series. The pinouts for the 74LS00 NAND has four gates inside and is shown below.



To use any of the gates in the chip, it must be attached to both power (+5 V) and ground.

1. Transistor Switch

Build the following circuit using the DMM to measure DC volts V_{CE}.

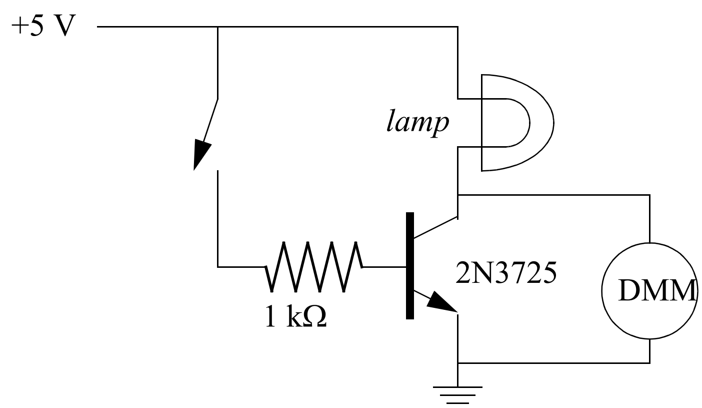


Figure 1: Transistor Switch

Close the switch and measure V_{CE} then measure the voltage across the base resistor. Use those measurements to determine I_C and I_B. Replace the 1 kΩ resistor with a 150 Ω resistor and repeat the measurement. Use a function generator set for square waves of 100 Hz that go from 0 to + 5 V to feed the base resistor, and observe the collector voltage with an oscilloscope. Measure the rise time and fall time for the transistor switch.

2. CMOS Analog Switch

A CMOS analog switch consists of two pairs on complementary MOSFETs where one pair is used to buffer and invert the control signal and the other pair is used to switch the signals through the source and drain of the MOSFETs. When V_{cont} is high (> 2.4 V) the switch is closed, if V_{cont} is at ground, the switch is open.

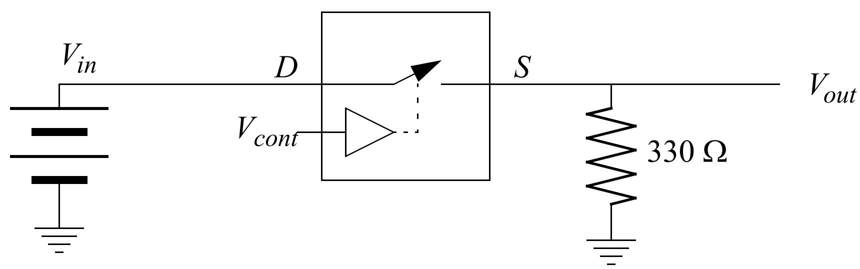


Figure 2: Analog Switch

Connect the ADG202A to power and ground and use one switch in the above circuit. Use V_{cont} = +5 V, and use a variable supply for V_{in}. Set V_{in} = + 10 V and measure V_{out}. Find the internal resistance of the switch by comparing V_{in} to V_{out} and treating the circuit as a voltage divider. Repeat the measurement of resistance with V_{in} = +2 V. Use a 1 MHz square wave from the TTL output to supply V_{cont}. Use V_{in} = +2 V, and compare V_{out} to V_{cont} with an oscilloscope. Find t_{on} which is the time from when V_{in} is 50% of its way on the rising edge to when V_{cont} is 90% of the way on its rising edge. Find t_{off} which is the time from when V_{in} is 50% of its way on the falling edge to when V_{cont} is 90% of the way on its falling edge.

3. TTL Logic Gate

Use an LED to build the following circuit. Test that the LED lights up when Vin is +5V and is off when Vin is at ground.

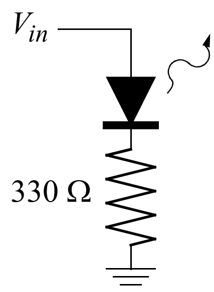


Figure 3: LED logic probe

Use a 74LS00 NAND gate to make the circuit in figure 3 (don't forget +5 V and ground).

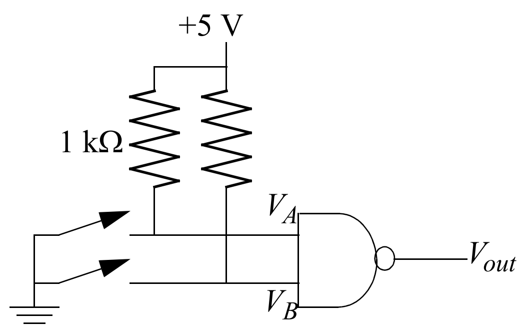


Figure 4: TTL NAND Gate

Make a truth table for all four combinations of switch settings, recording the voltage levels with a DMM for V_A, V_B, and V_{out}, and measure the logic levels with an LED logic probe. How does V_{out} change when the logic probe is attached? Switch both inputs to ground and place a 1 MΩ resistor to ground. Measure V_{out} with the DMM and calculate I_{out}. Repeat the measurement for resistors of 10 kΩ, 1 kΩ, 470 Ω, 220 Ω, and 100 Ω. Plot I_{out} vs. V_{out}.