Silicon Tungsten Calorimetry

David Strom
University of Oregon

- Design Consideration
- Silicon Detector Design
- Electrons and Noise
- Mechanical Design
- Timing resolution
- Plans and lab activity
- Si-W Mechanical Design

Si-W work – personnel and responsibilities

M. Breidenbach, D. Freytag, N. Graf, G. Haller,O. Milgrome SLAC	R. Frey, D. Strom UO	V. Radeka BNL
Electronics, Mechanical Design, Simulation	**Si Detectors**, Mechanical Design, Simulation	**Electronics**

Primary ECAL Design Requirements

- Excellent separation of γ's from charged particles
  Efficiency $> 95\%$ *for energy flow*

- Good reconstruction of $\pi^{\pm}$, detection of neutral hadrons

- Reasonable EM energy resolution ($< 15\%/\sqrt{E}$)

- Reconstruct τ's and measure polarization (separate π, ρ, a_1, e's)

- Reconstruct Bhabhas and deconvolve luminosity spectra
  Position resolution $\sim 100\mu m$*, bias* $\sim 25\mu m$ *in endcap*

Secondary ECAL Design Requirements

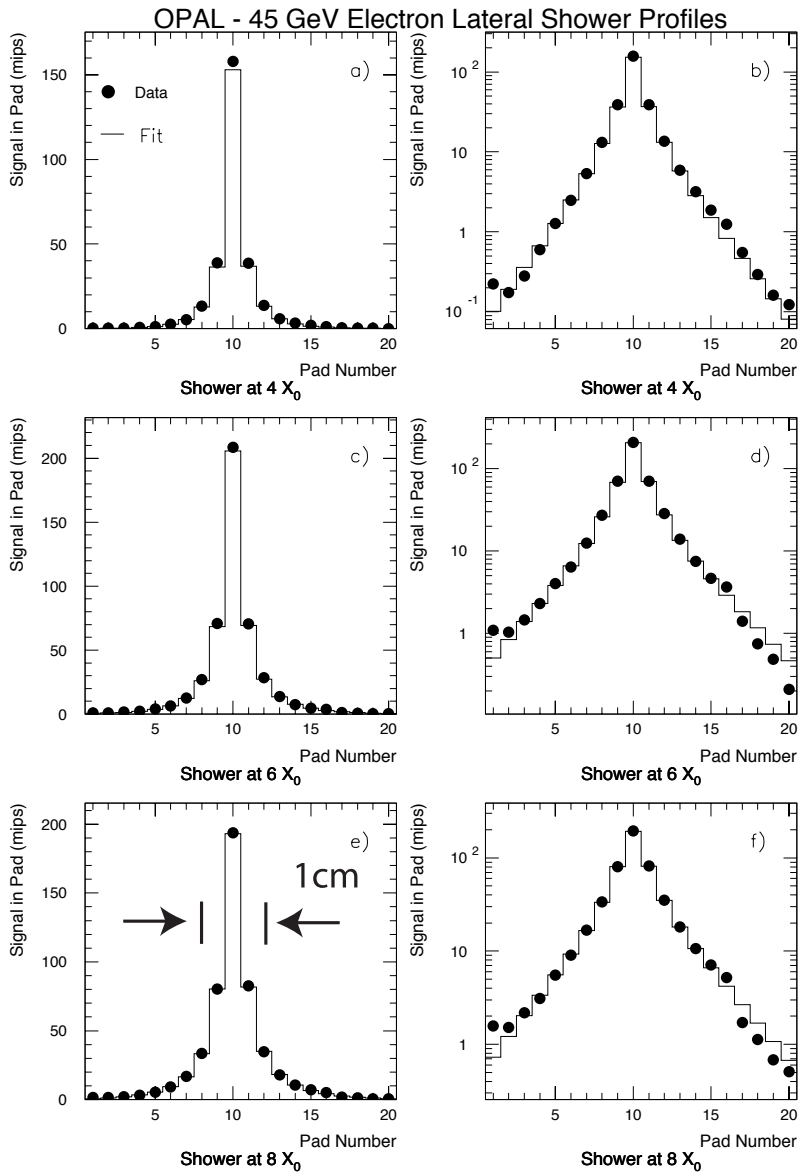
- Excellent electron identification in jets (tag and b/c quarks)
- Partial reconstruction of b/c hadrons in jets
- Good γ impact resolution for long lived SUSY neutrals
  $\sim 1\ cm$
- Good background immunity
  - Bunchlet identification
  - High granularity

SiW Design Consideration

- Transverse shower size scales with Molière radius
  (9mm in pure W,
  16mm in pure Pb)
  ⇒ *Minimize gaps between layers of absorber*
  ⇒ *Use a high purity W alloy*

- Sample between 1/2 and 2/3 of X_0 (1.75mm to 2.5mm of W)

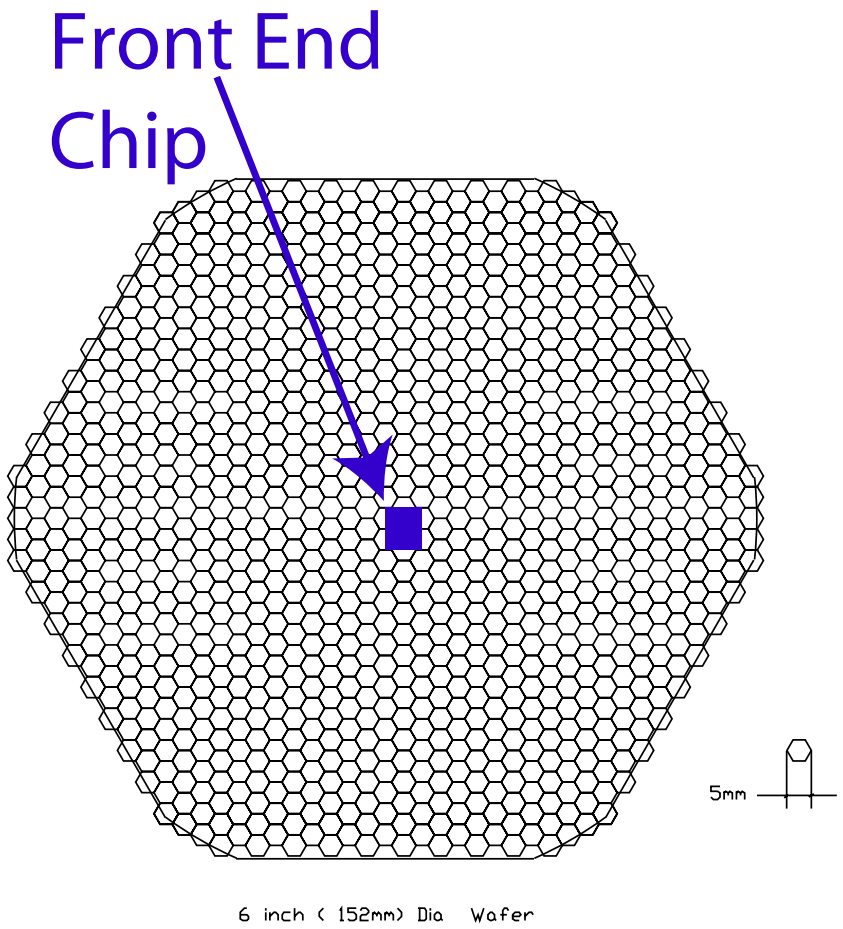
- Allow for detector segmentation at a fraction of the Molière radius
  ⇒ *Use* $\sim 5mm$ *pads*



$1\,X_0$ sampling, 2.8 mm gap

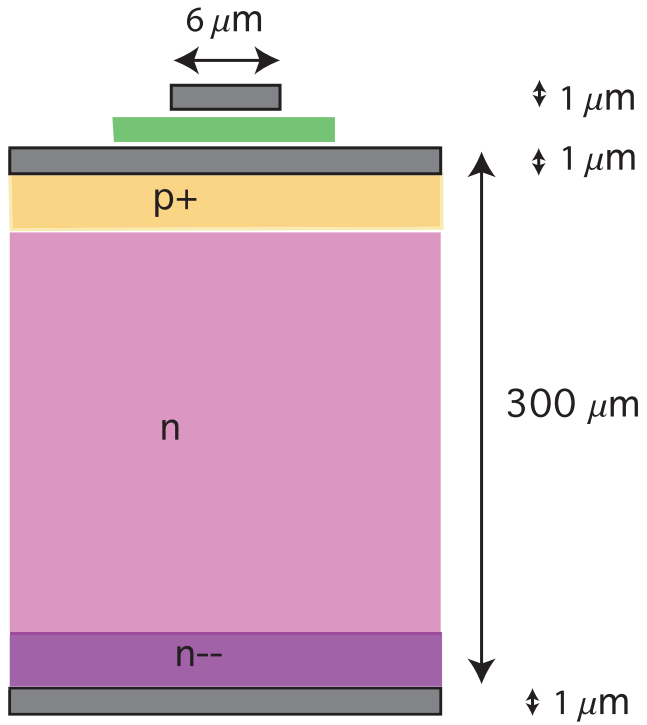
Silicon Concept

- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of front end chip
- May want different pad layout in forward region



Silicon Design Details

- DC coupled detectors
- Two metal layers
- Keep Si design as simple as possible to reduce cost
- Cross talk looks small with current electronics design



Electronics Design

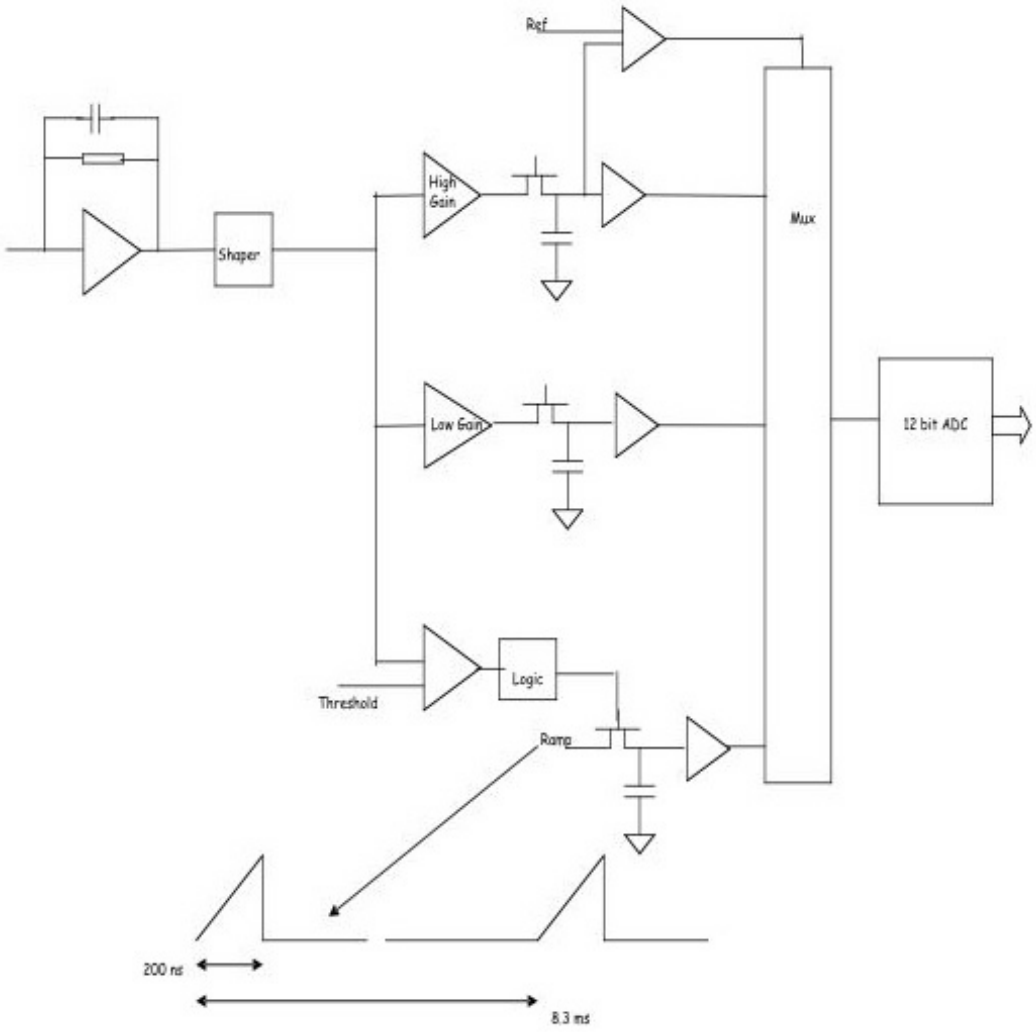
- Chip area driven by feedback capacitor on charge integrator and 3V supply.
  Need 2000 MIP (8 pC) dynamic range for 500 GeV electrons.
  $\Rightarrow$ 10pF feedback capacitor needed

- New design samples integrated (τ = 200ns) signal after 1μs for each bunch train
  Lowers cross talk, little gain variation with bunch-let number

- Timing at the 10ns level should be possible

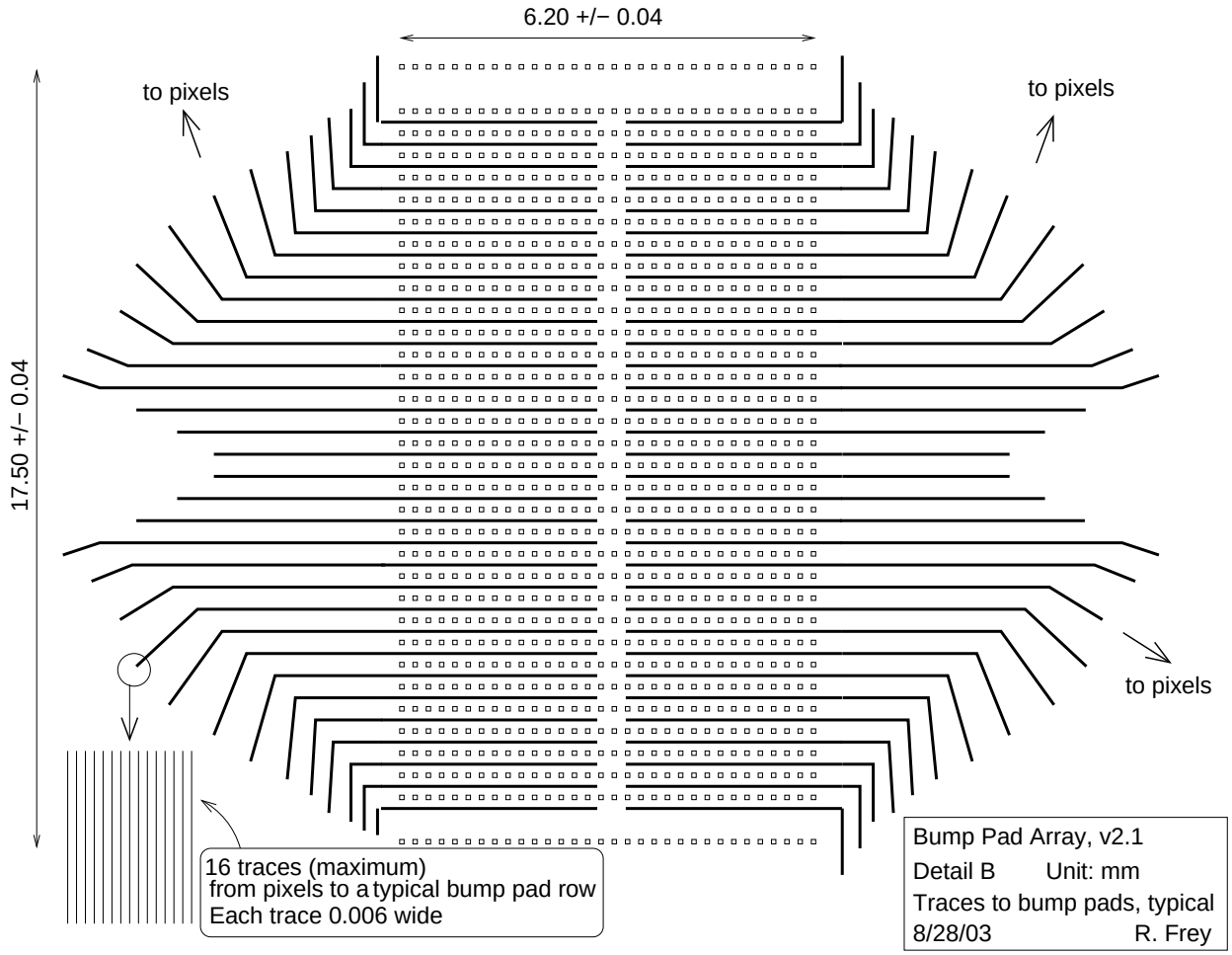
- Current in input transistor pulsed
  duty cycle $< 10^{-3}$ *0.1mW/ch*

- Currently estimating chip area and power needed for digital section



Si Prototypes

- Design completed
  Provisional grid spacing for bump-bonding



Si Prototype properties – leakage current and noise

• Radiation damage to detectors is probably dominated by neutrons, $\sim 10 \times 10^{10}/\mathrm{cm}^2$

$$\Rightarrow < 10\mathrm{nA} \text{ /pixel leakage current}$$

• Expect typical leakage current at start of life $<$ 1nA/pixel

• Noise from leakage current at end-of-life for 1μs sampling time (can be adjusted) and DC coupling scheme is $<$ 350 electrons

• Largest source of electronics noise will be front-end input transistor, noise scales as

$$\frac{C_{in}}{\sqrt{\tau} I^{1/4}} \propto \frac{C_{in}}{\sqrt{\tau} \text{power}^{1/4}}$$

• Present design has noise:

$$\sim 20 - 30 e/\text{pf}$$

For most channels the value of C_{input} is dominated by stray capacitance of the trace connecting the pixels to the electronics:

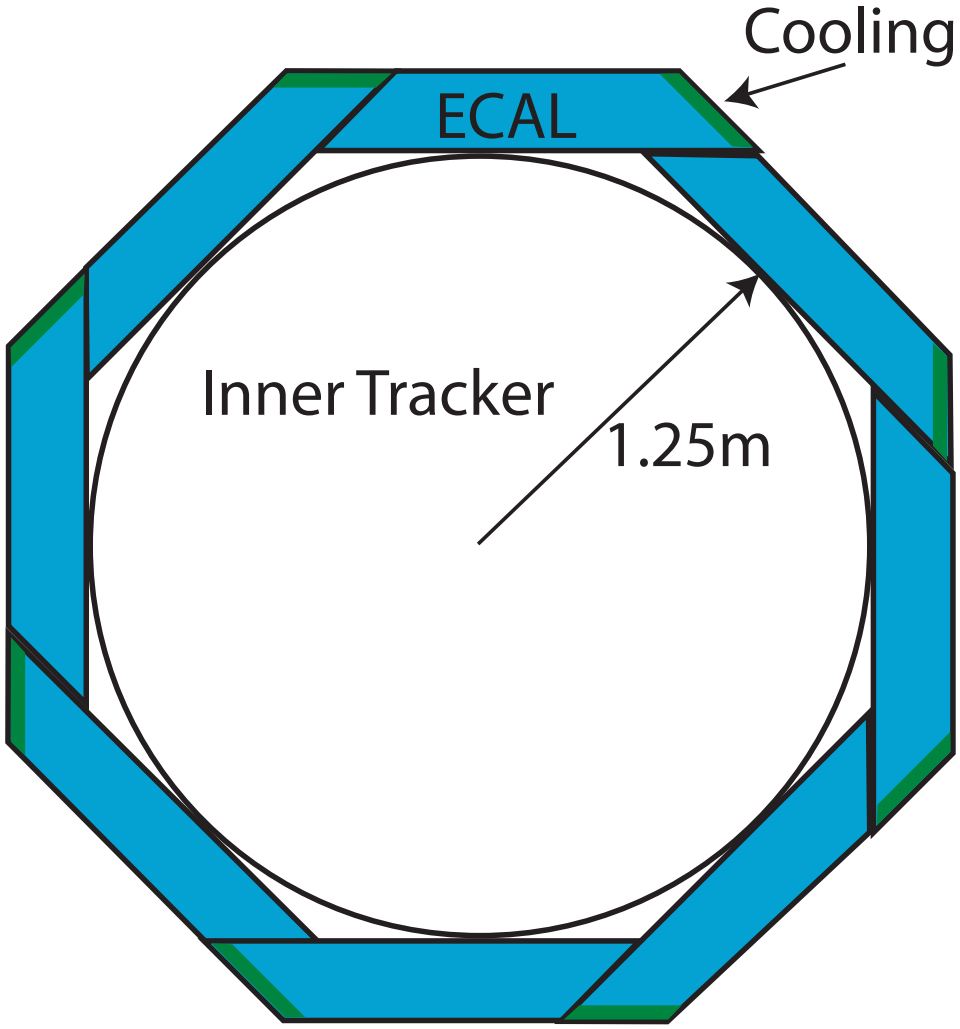
$$C_{input} \sim 5.7\text{pF(pixel)} + 12\text{pF(trace)} + 10\text{pF(amp)} \sim 30\text{pF}$$

$$\longrightarrow \sim 1000 \text{ electrons noise (c.f. 24,000 from MIP)}$$

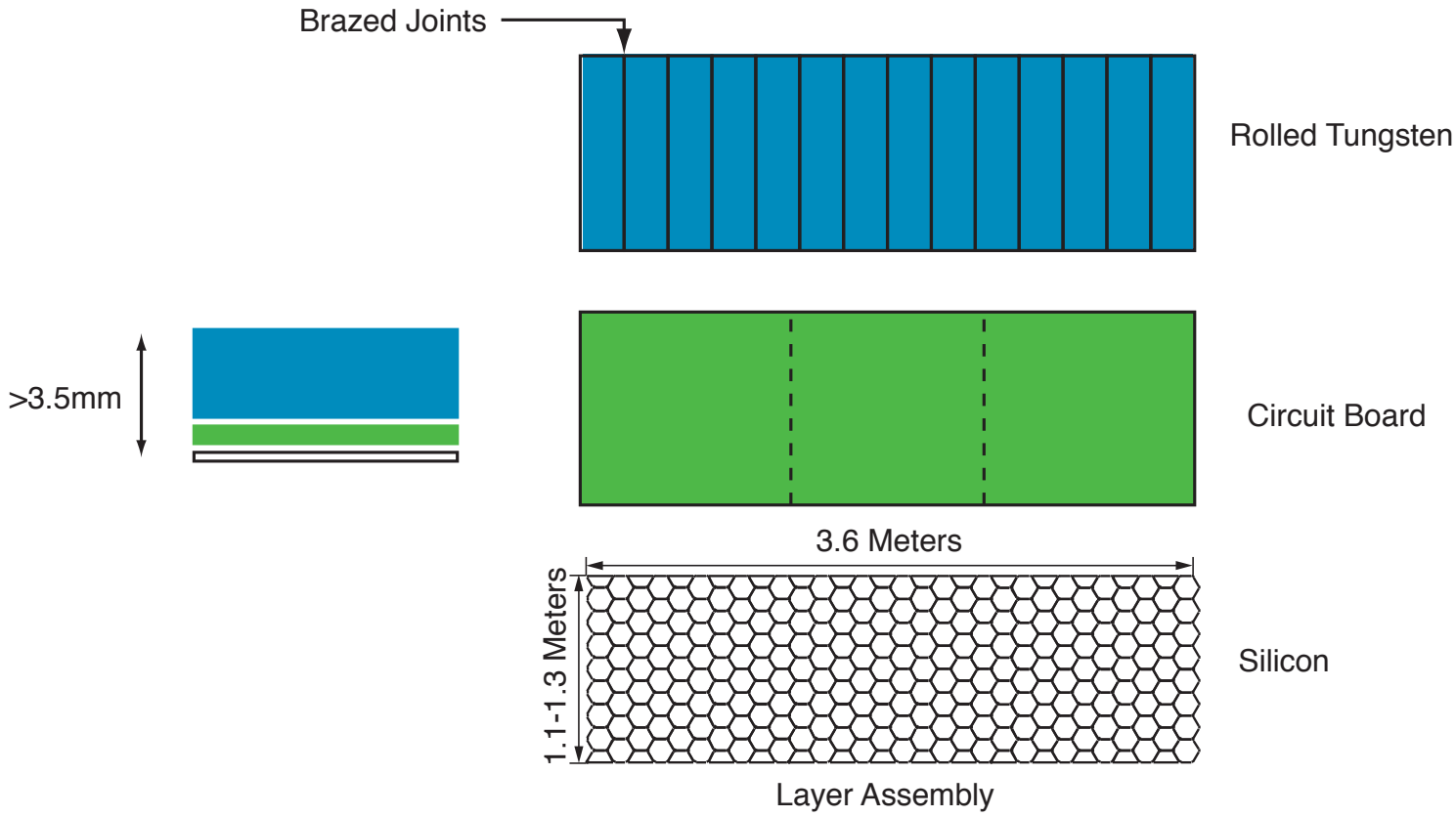
• Analog power consumption will probably be driven by timing requirements (under investigation)

Fitting it all together

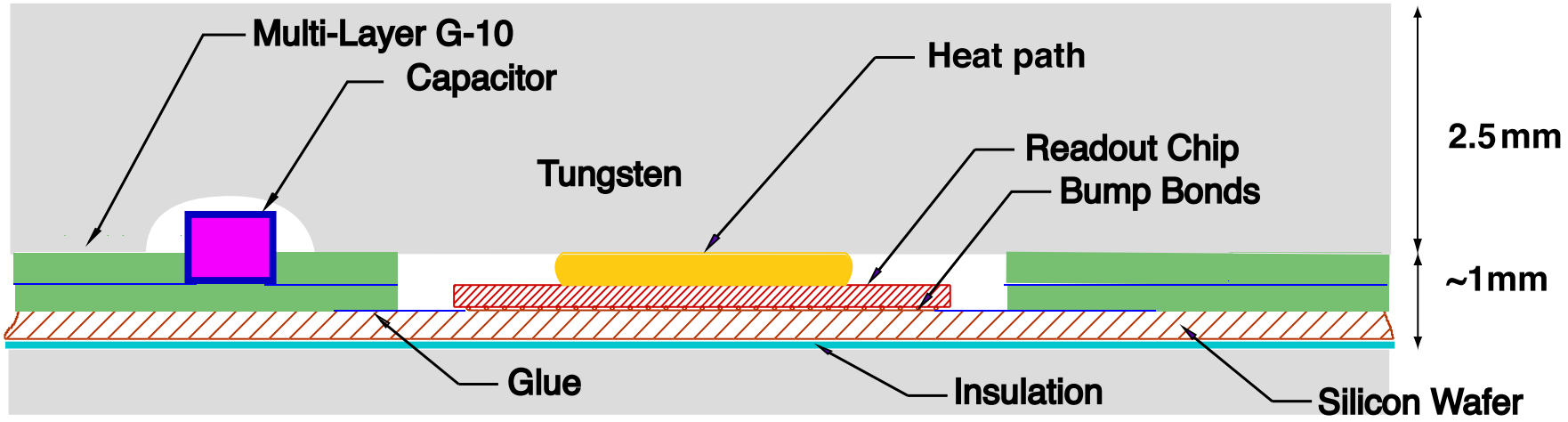
- Cartoon of possible barrel calorimeter configuration
- Assume heat flows along tungsten and/or copper heat sink to cooling water (green)
- Longest path for heat flow < 1.4m



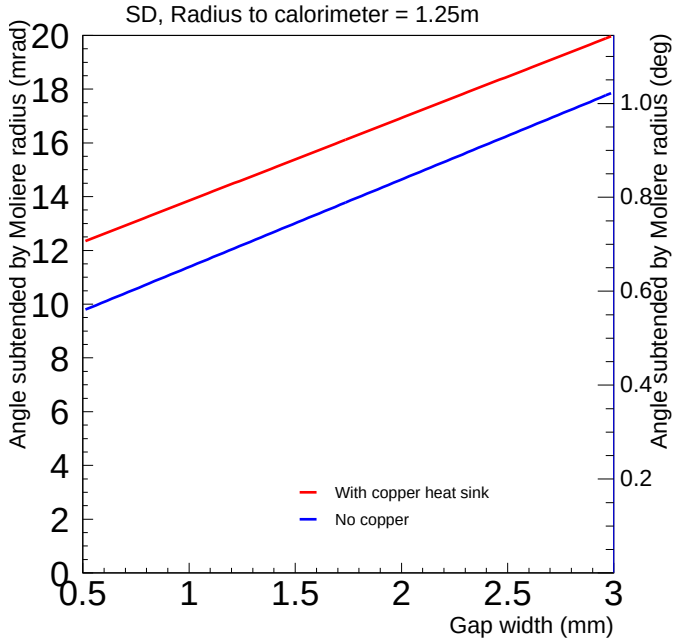
Layout of Individual calorimeter layers:



Critical parameter: minimum space between tungsten layers.



Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
+1mmCu	6.4mm	17mm



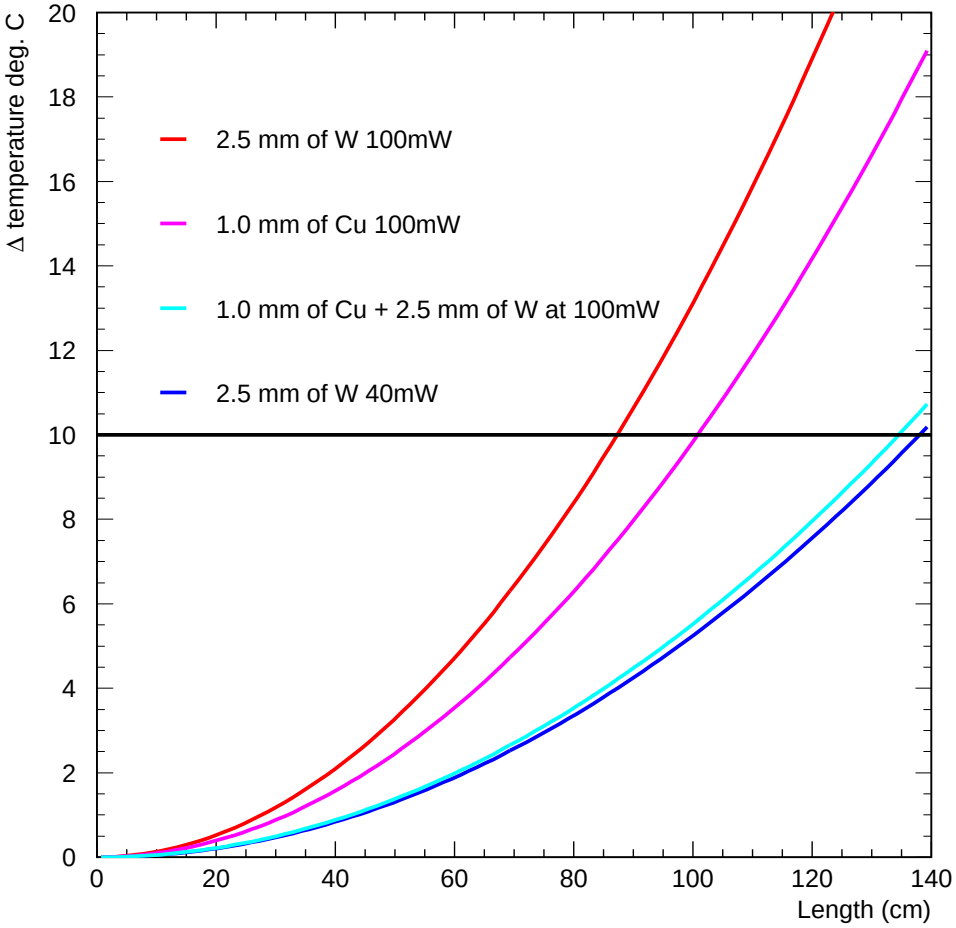
Heat flow

Back of the envelope calculation of change in temperature:

- Thermal Conductivity of W alloy 120W/(K-m)
- Thermal Conductivity of Cu 400W/(K-m)

Need to reduce heat to below 100mW/wafer.

Physical model test in progress



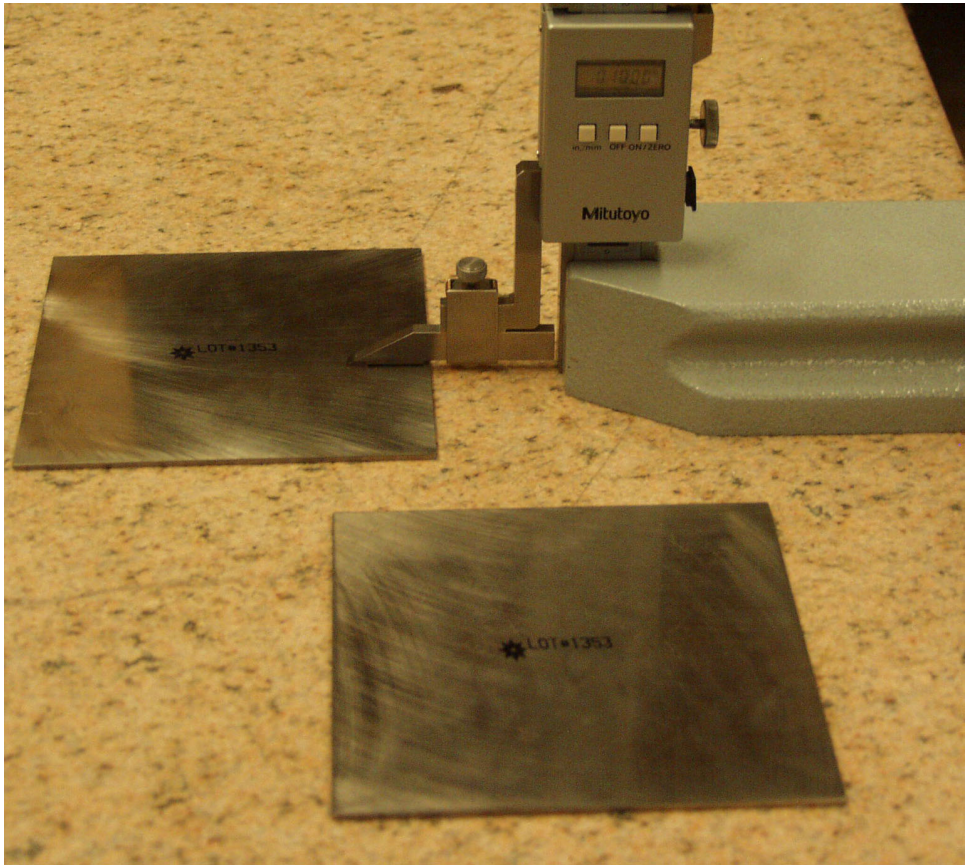
Prototype Tungsten Pieces

- OPAL tungsten ground to size (almost more expensive than tungsten itself!)

- Prototype rolled pieces (92.5% W) look fine (some grinding still needed)

- Quality better than OPAL

- 1 m long pieces possible



Summary of Granularity – *Most important figure of merit*

- With 92.5% W and 1 mm gap we can have a Molière radius of

$$\sim 14\,\mathbf{mm}$$

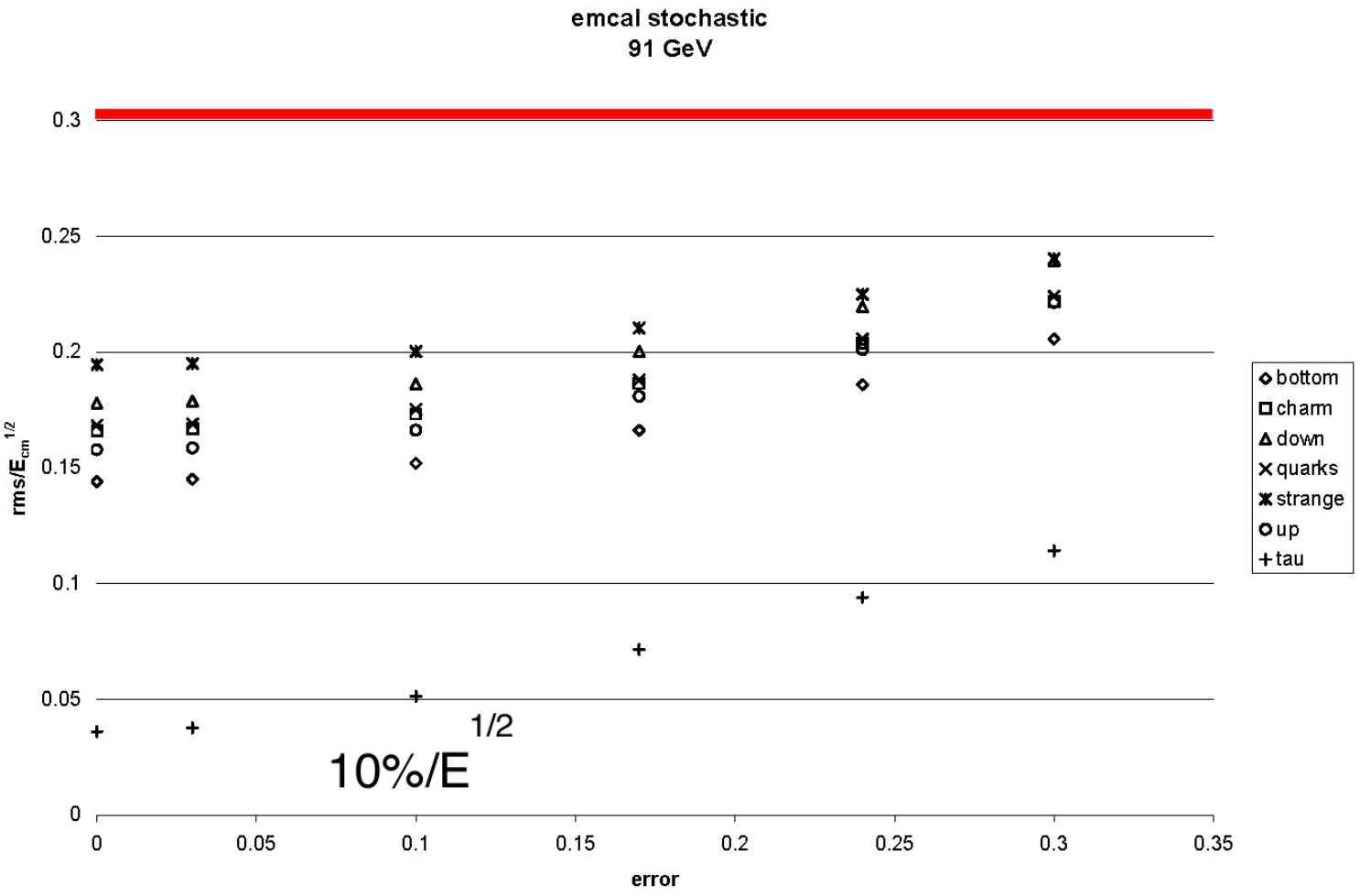
which has an angular size of **11 mrad** at 1.25 m

$\Rightarrow$ provided we can keep the power down to **40 mW** wafer

- *This will be challenging, but may be possible*

What about energy resolution $\Rightarrow$

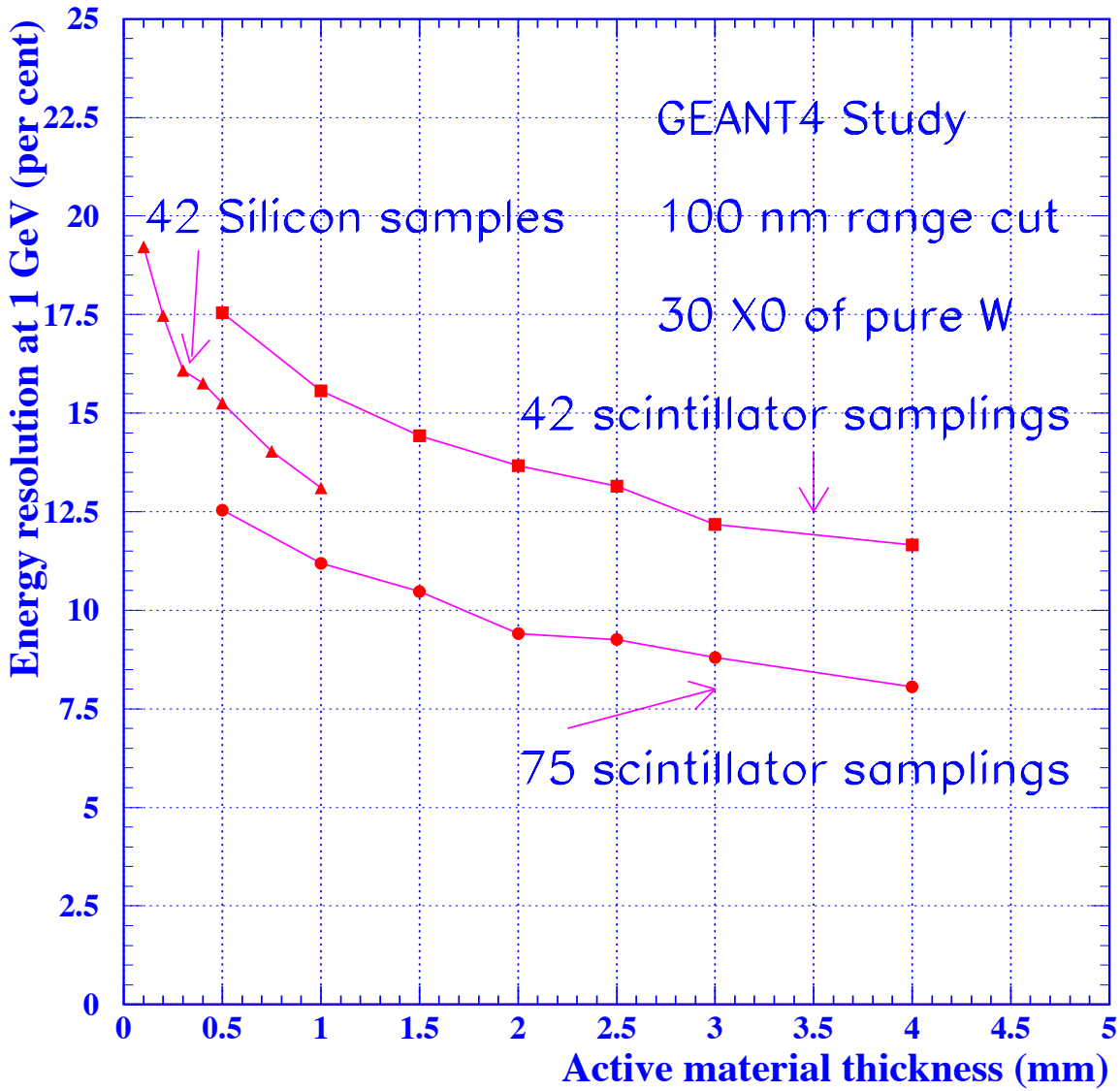
Jet energy resolution will suffer if we give up too much sampling (Graham Wilson's plot):



Assumes $\sigma_{p_t}/p_t^2 = 5 \times 10^{-5}$, HCAL res $50\%/\sqrt{E} \oplus 4\%$

Geant 4 simulation of energy resolution from Graham Wilson

- 1 GeV photons
- 0.1 μm range cuts
- 42 and 75 layers of W
- Si apparently benefits from subMIP energy deposits – can we see this in a real detector?

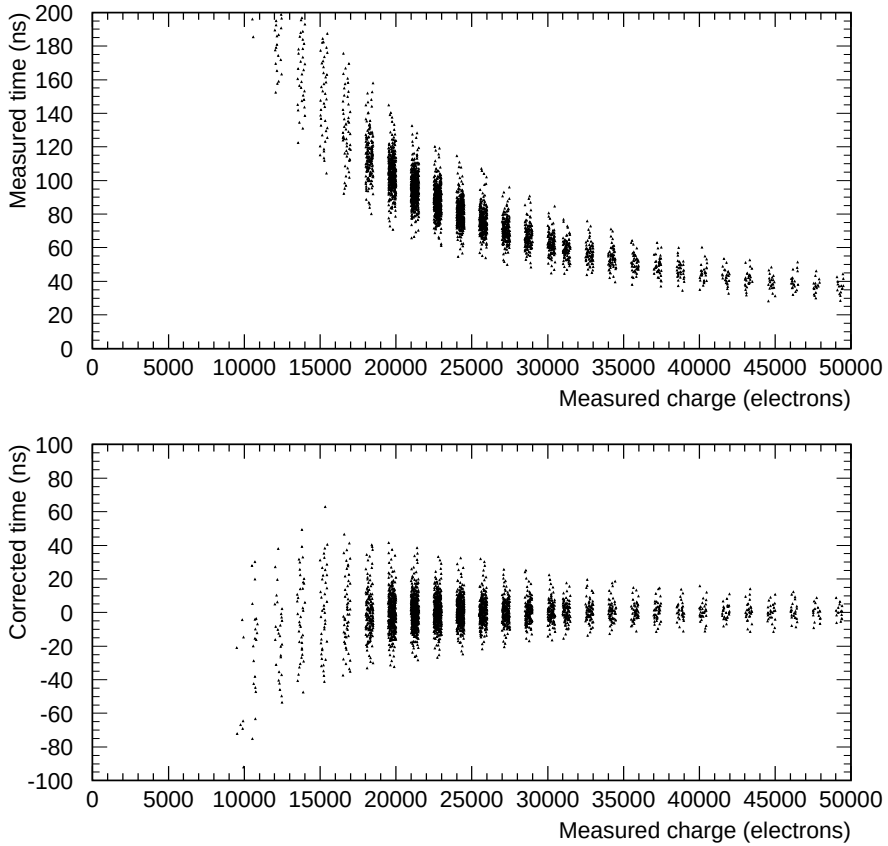


Toy Monte Carlo Studies of Timing Resolution for 30 Samples

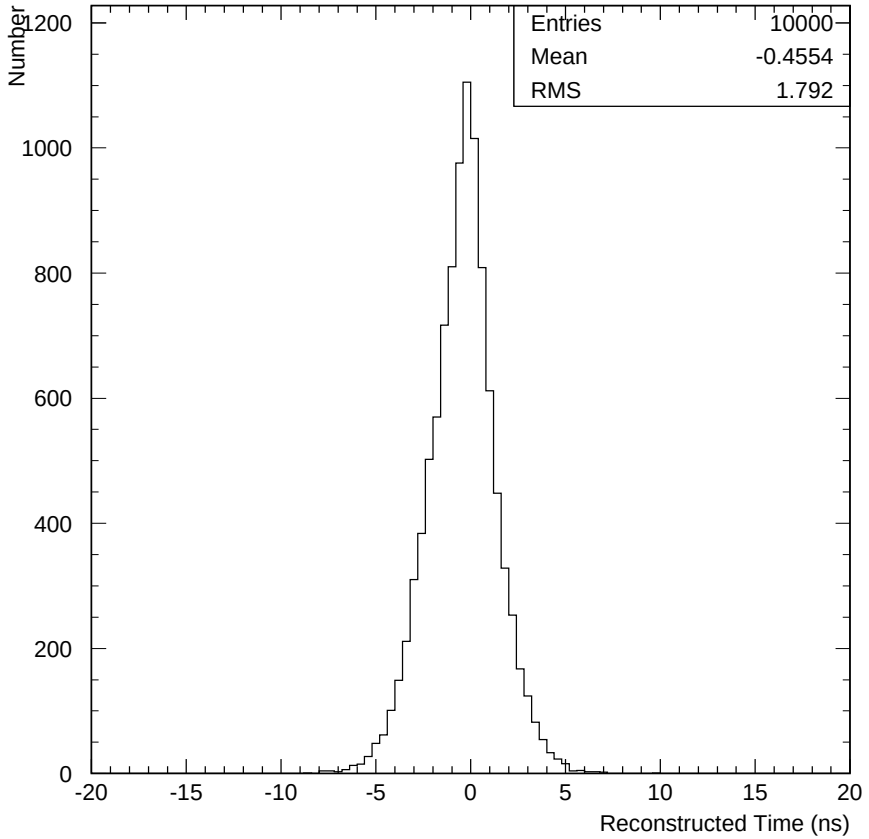
Assumptions – wild guesses – (waiting for real electronics model):

- Timing circuit and charge amplifier have the same integration time of 200 ns.
- Input FET has $g_m = 2$mS
- Excess noise is equal to FET noise
- Includes reasonable distribution of capacitances from second metal layers
- Threshold is set at 8000 electrons (Typical noise $\sim$ 1000 electrons)
- 5% gitter channel-to-channel, 1% common mode gitter in thresholds
- Charge granularity of 0.061*1MIP
- Channel-to-channel leakage current variations perfectly corrected

Sample Timing Results



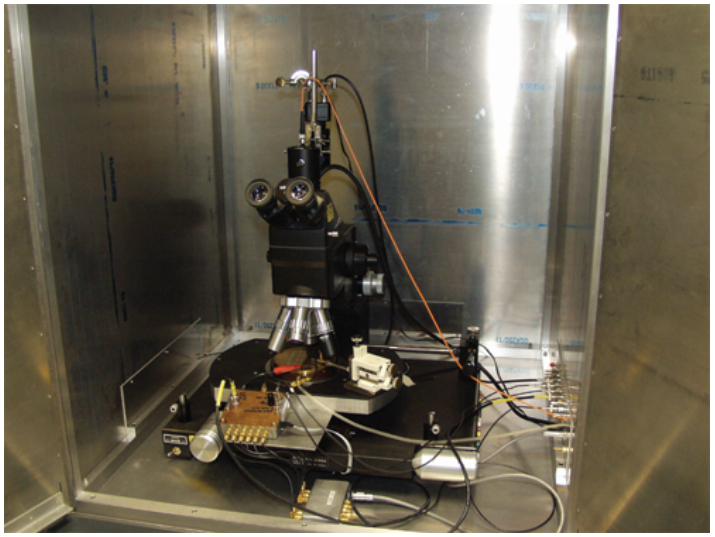
Time versus charge for mips



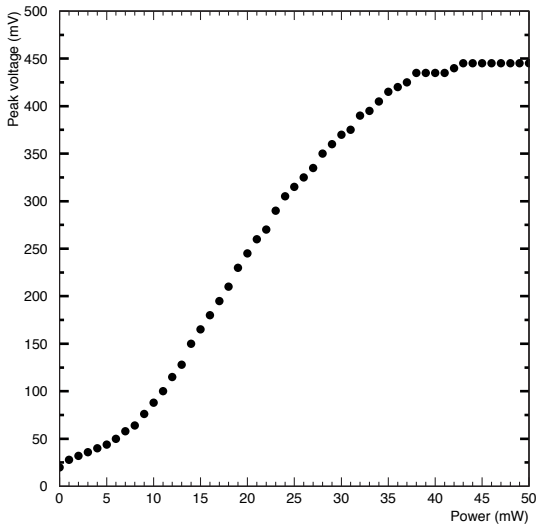
30 Sample average time

Practice with 6x6 1cm^2 cell detectors:

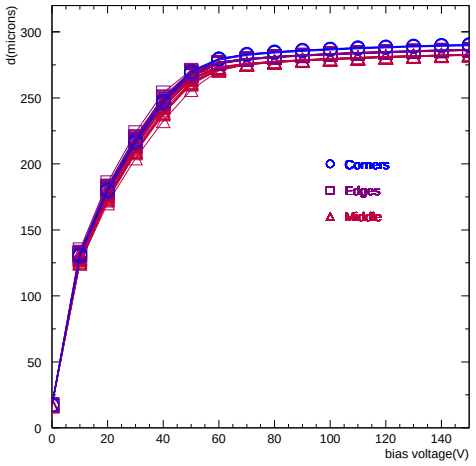
Probe station



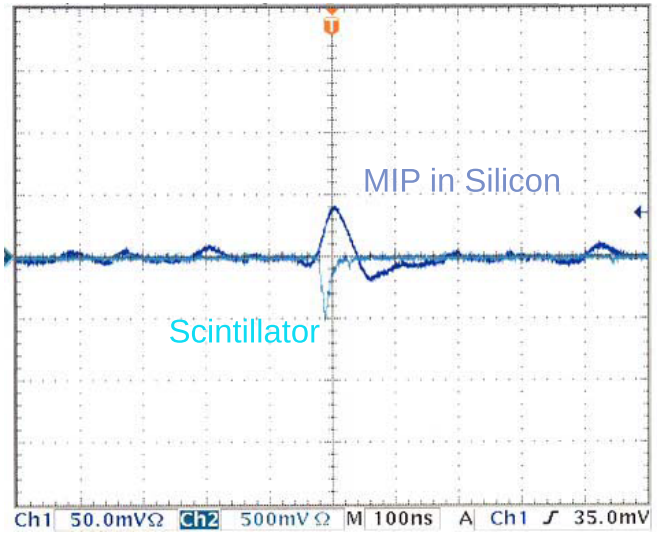
IR laser



Depletion depth from CV curve



MIP with scintillator



Si-W status

- Design of first silicon detectors complete
  $\Rightarrow$ Prototypes will arrive in early '04

- Electronics rough draft complete
  $\Rightarrow$ Expect to be ready for submission in early '04

- Mechanical conceptual design started
  $\Rightarrow \sim$ 1mm gap between layers without a copper heat sink may be possible
  $\Rightarrow$ Gap size depends crucially on power consumption

Si-W Near Term Plans

- Produce prototype electronics – early next year
- Test bump bounding electronics to detectors in '04
- Ready for Test Beam in '05
- Confirm thermal model and explore best coupling method of chips to absorber
- Simulation job list:
  - Optimize sampling for energy resolution
  - Compare GEANT 4 /EGS and data on Eres versus silicon thickness
  - Optimize pixel layout
  - Would more granularity help?
  - How sensitive is energy flow to Molière radius?