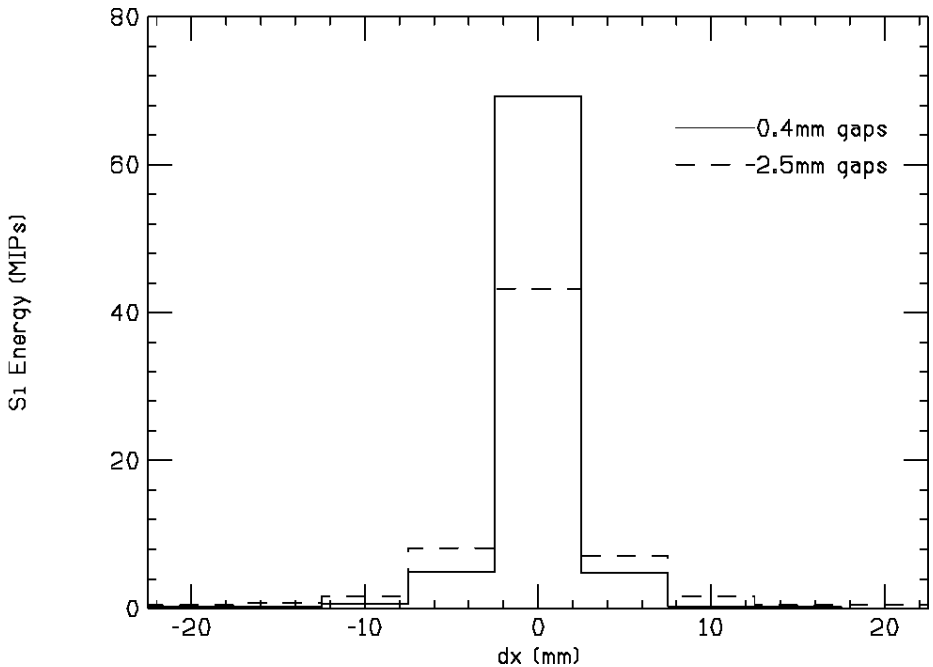
ECal Items

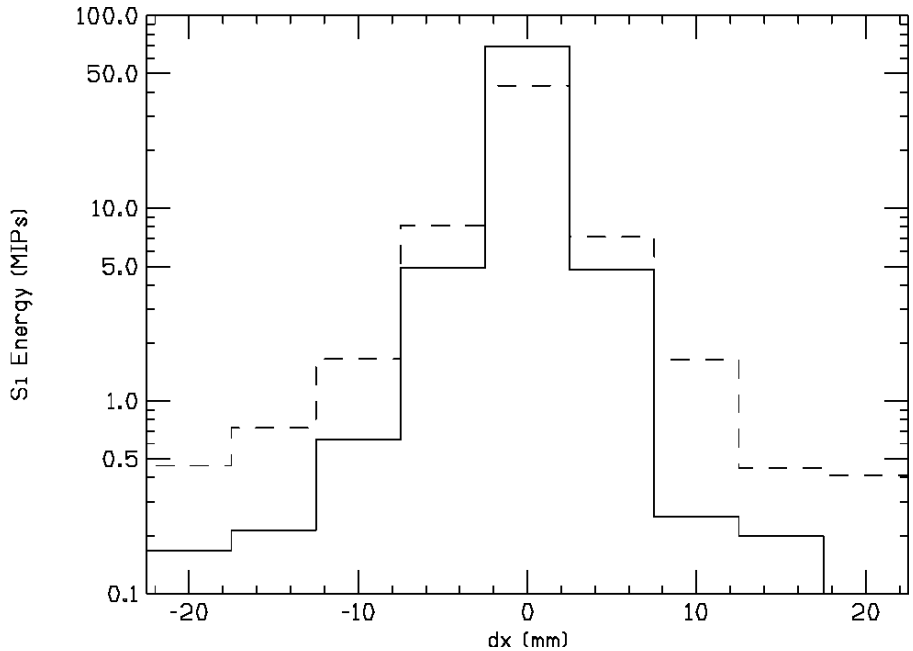
Ray Frey

- ECal Optimization Issues
  - Longitudinal Sampling
  - Radius
- Si/W Brief Status
- Upcoming Meetings

Effective Moliere radius

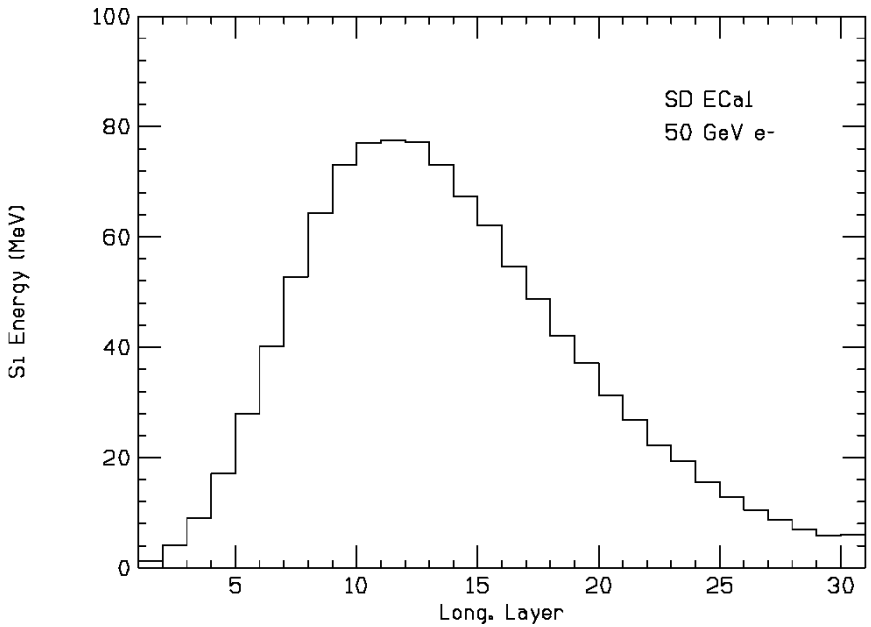
- Standard SD: 5x5 mm^2 pixels with (1) 0.4mm or (2) 2.5mm readout gaps.
- 10 GeV photons; look at layer 10



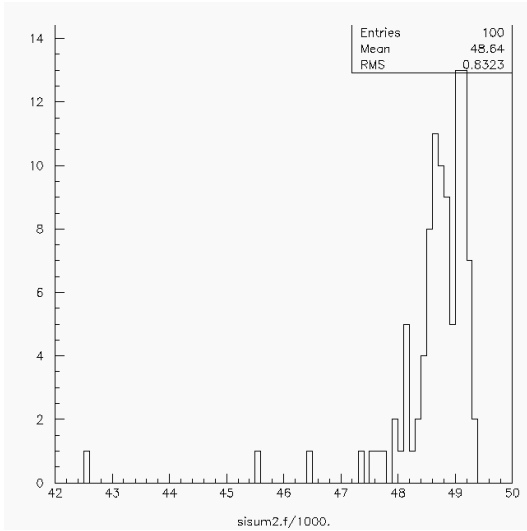


Standard SD: 30 Layers, 21 X_0.

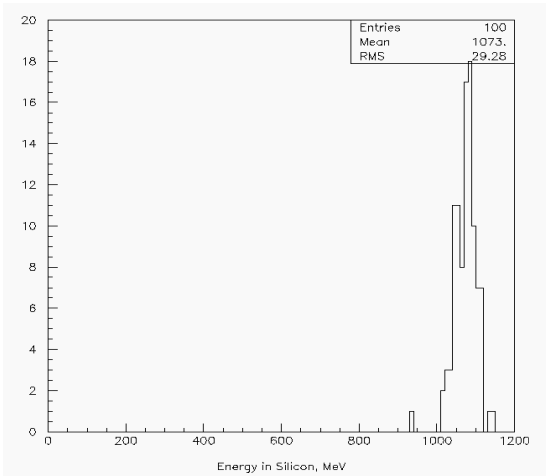
50 GeV electrons



Total Absorbed Energy

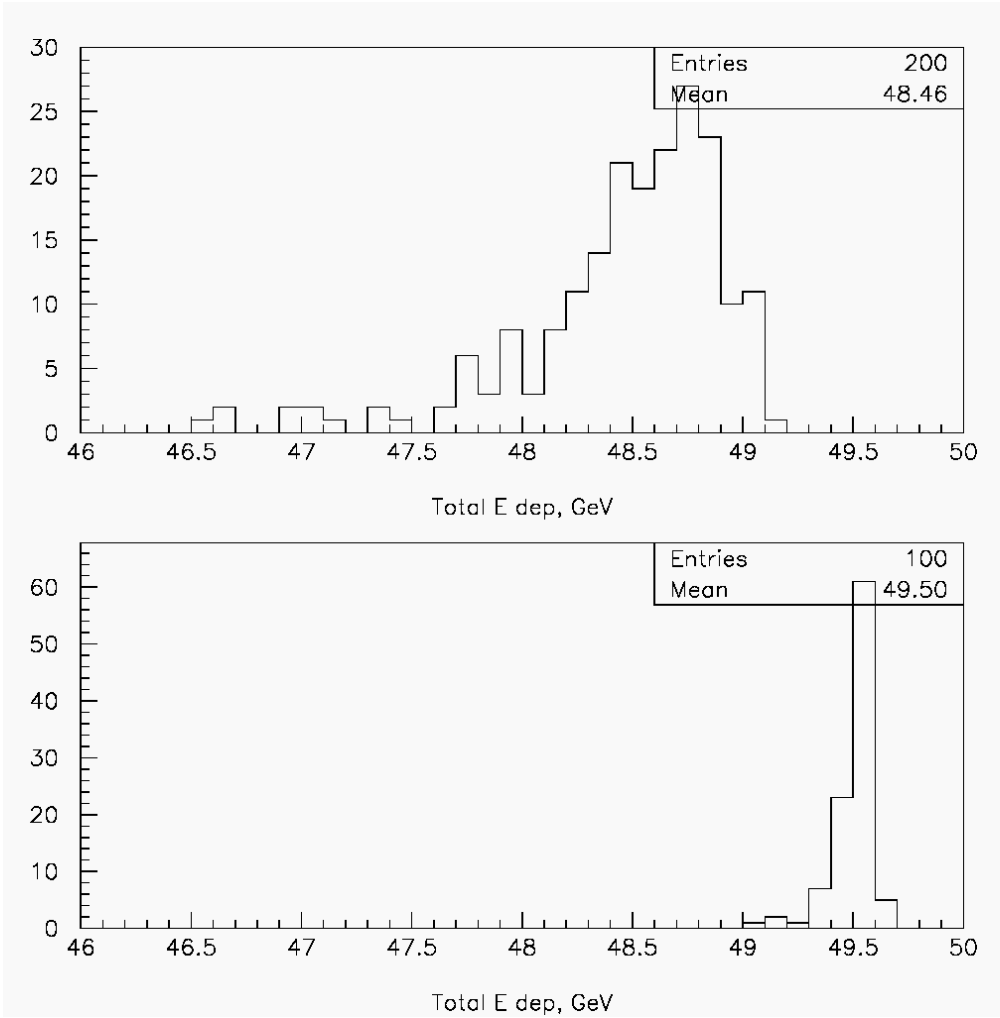


Total Energy in Si



$$\sigma_E / E \approx 0.16 / \sqrt{E}$$

Alternative Longitudinal Sampling Configurations



50 GeV electrons

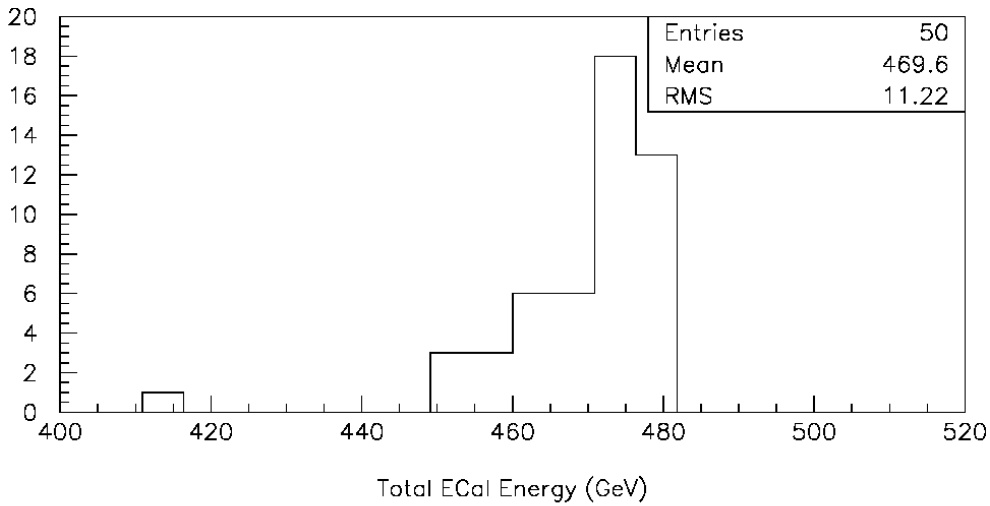
SD: 30 x 5/7 X_0 (21.4)

SD vB: 20 x 5/7 X_0 + 10 x 10/7 X_0 (28.6)

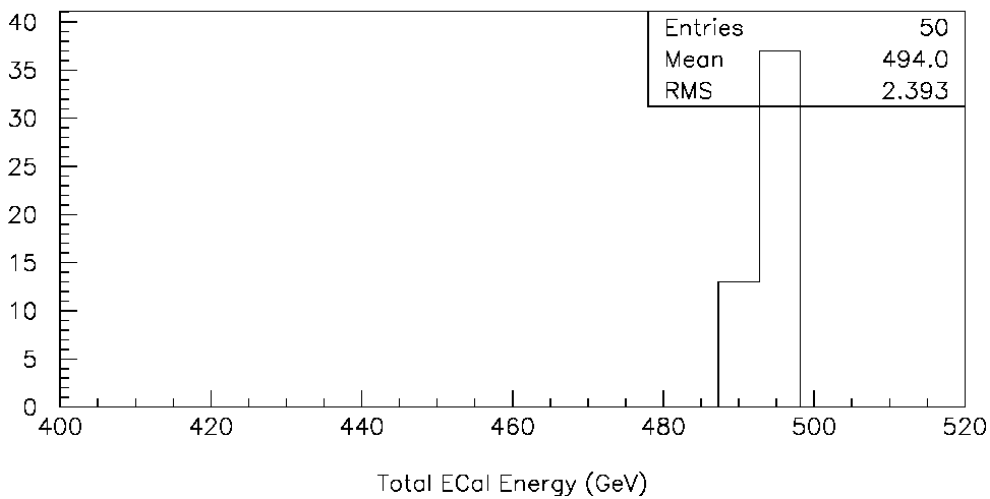
- better containment
- poorer sampling

Alternative Sampling (contd.)

500 GeV electrons



SD: 30 x 5/7 X_0

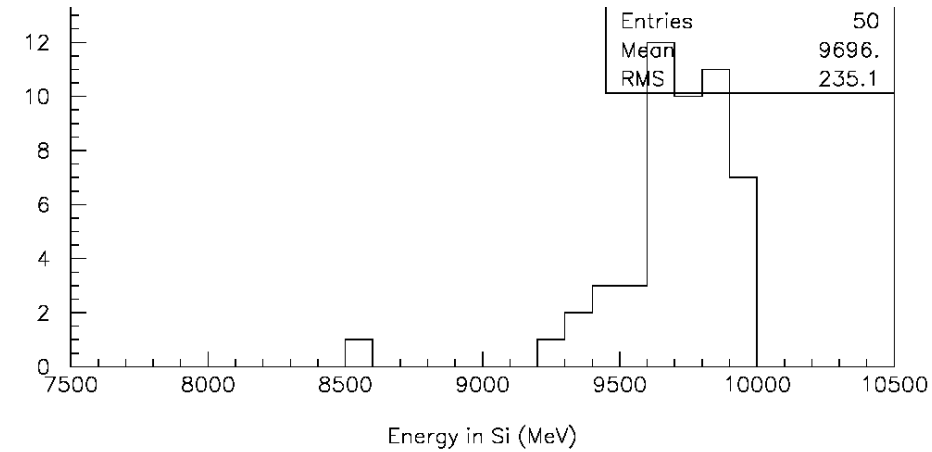


SD vB: 20 x 5/7 X_0 + 10 x 10/7 X_0

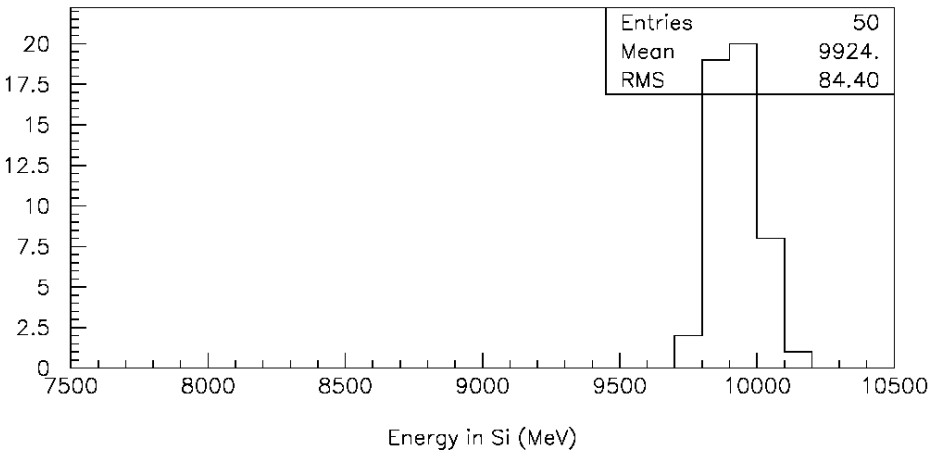
Alternative Sampling (contd.) resolution

500 GeV electrons

Energy in Si



SD: 30 x 5/7 X_0



SD vB: 20 x 5/7 X_0 + 10 x 10/7 X_0

ECal Optimizations

- Recall that in our design, transverse seg. Is nearly independent of cost. EM showers are *very* narrow, esp. not past shower max.
- Is there a downside to going to a deeper config., as vB ?
- MB shows that at B=4T, cost does not vary so strongly with ECAL radius. Better EFlow at R_{in}=1.7m ?
- Remove ECal-HCal gap
- (Put W behind layer 30 ?)

W/Si Progress

- Si detectors
  - Have drawings (almost bid) from one of two vendors
  - At this point, need LCRD money to advance
- Readout Electronics
  - A first design of readout frontend (D. Freytag, SLAC)
    - seems to meet specs for performance
    - power seems OK
    - Layout looks OK for chip footprint
  - ASIC specifications document
- Preparing for first round of prototypes and tests
  - B field
  - Bump bonding