Progress on Silicon-Tungsten Calorimeter for SD

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- Design Consideration
- Silicon Detectors
- Electronics
- Some Mechanical Details

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Primary ECAL Design Requirements

- Excellent separation of γ's from charged particles
  Efficiency $> 95\%$ *for energy flow*

- Good reconstruction of $\pi^{\pm}$, detection of neutral hadrons

- Reasonable EM energy resolution ($< 15\%/\sqrt{E}$)

- Reconstruct τ's and measure polarization (separate π,ρ, a_1, e's)

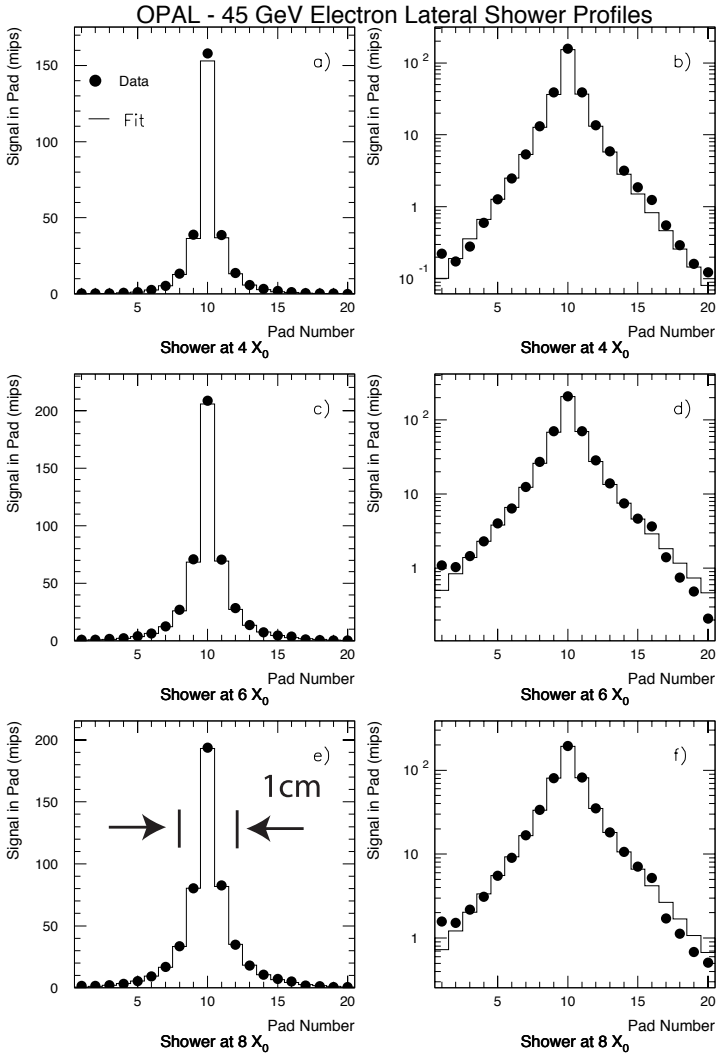
- Reconstruct Bhabhas and deconvolve luminosity spectra
  Position resolution $\sim 100\mu m$*, bias* $\sim 25\mu m$ *in endcap*

Secondary ECAL Design Requirements

- Excellent electron identification in jets (tag and b/c quarks)
- Partial reconstruction of b/c hadrons in jets
- Good γ impact resolution for long lived SUSY neutrals
  $\sim 1\ cm$
- Good background immunity
  - Bunchlet identification
  - High granularity

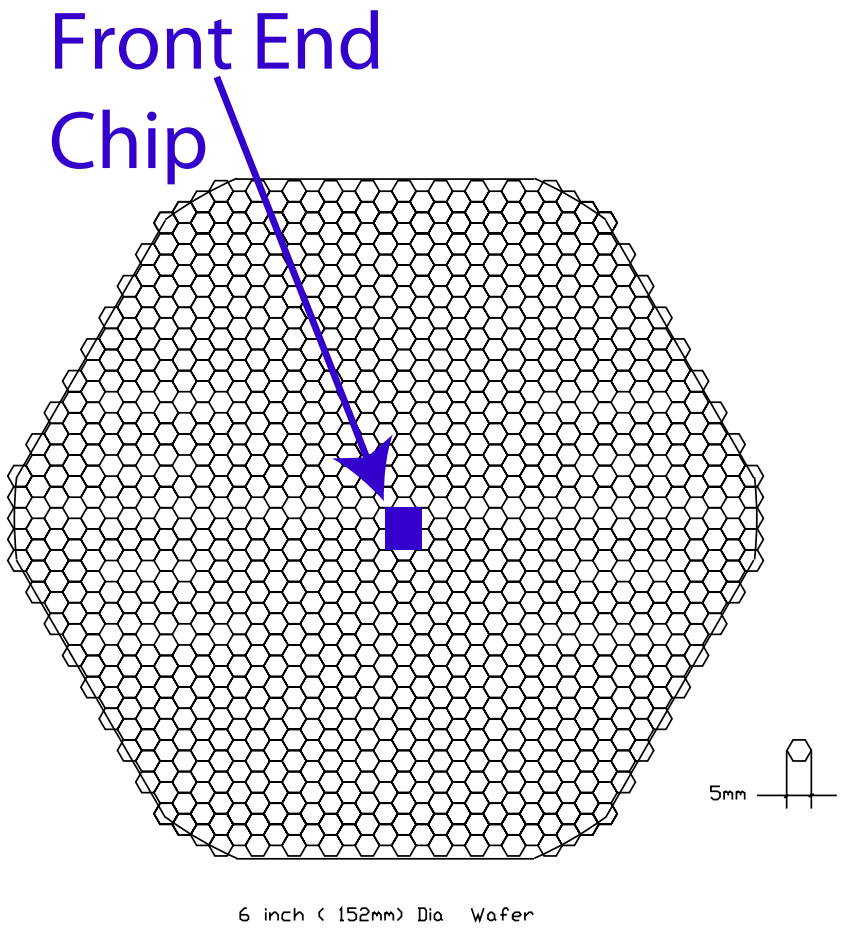
SiW Design Consideration

- Transverse shower size scales with Molière radius (9mm in pure W, 16mm in pure Pb)
  $\Rightarrow$ *Minimize gaps between layers of absorber*
  $\Rightarrow$ *Use a high purity tungsten alloy*
- Sample between 1/2 and 2/3 of X_0 (1.75mm to 2.5mm of W)
- Allow for detector segmentation at a fraction of the Molière radius $\Rightarrow$ *Use* $\sim 5mm$ *pads*



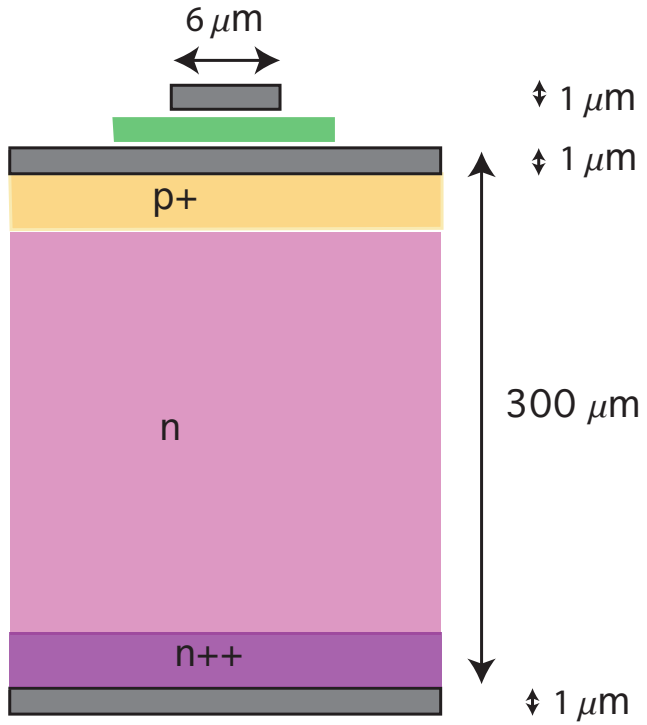
Silicon Concept

- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of front end chip
- May want different pad layout in forward region



Silicon Design Details

- DC coupled detectors
- Two metal layers
  Could a design with only one work?
- Keep Si design as simple as possible to reduce cost
- Cross talk look small with current electronics design



Electronics Design

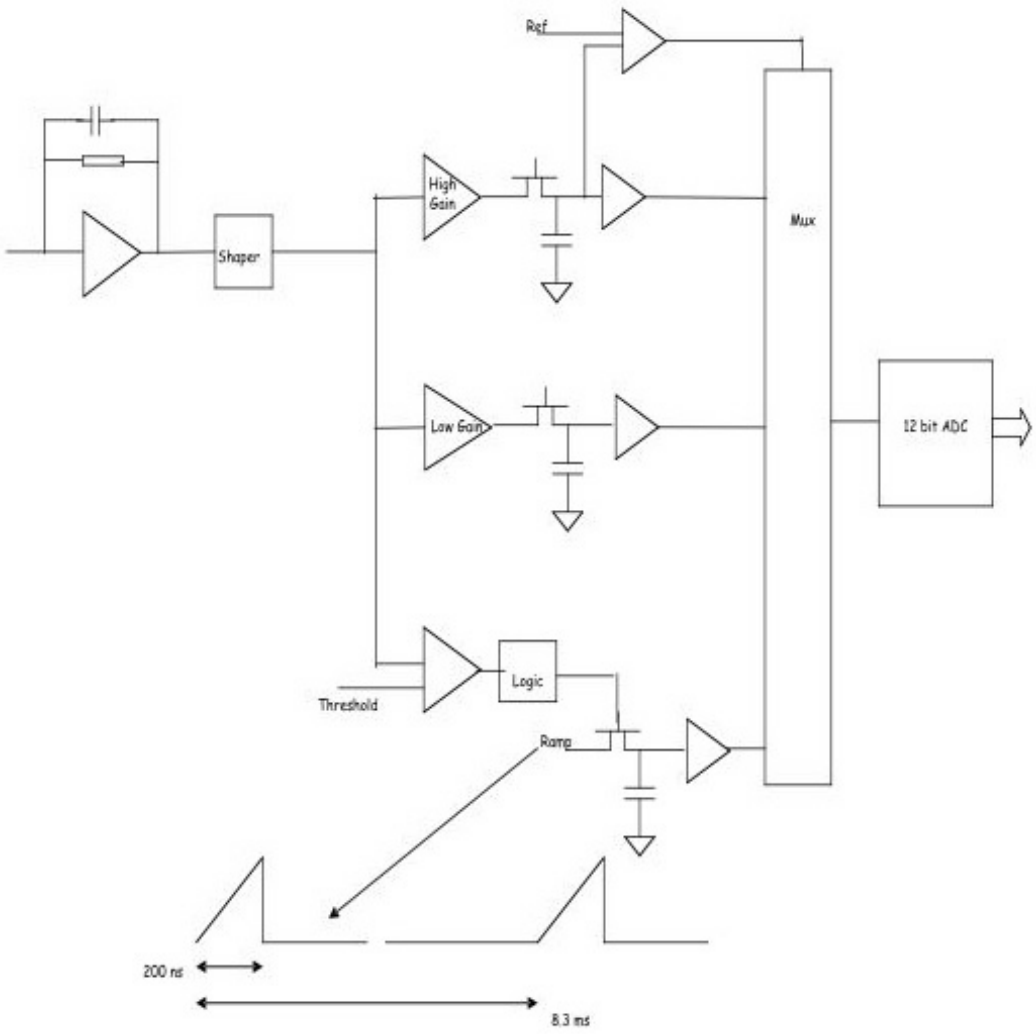
- Chip area driven by feedback capacitor on charge integrator and 3V supply.
  Need 2000 MIP (8 pC) dynamic range for 500 GeV electrons.
  $\Rightarrow$ 10pF feedback capacitor needed

- New design samples integrated (τ = 200ns) signal after 1μs for each bunch train
  Lowers cross talk, little gain variation with bunchlet number

- Timing at the 10ns level should be possible

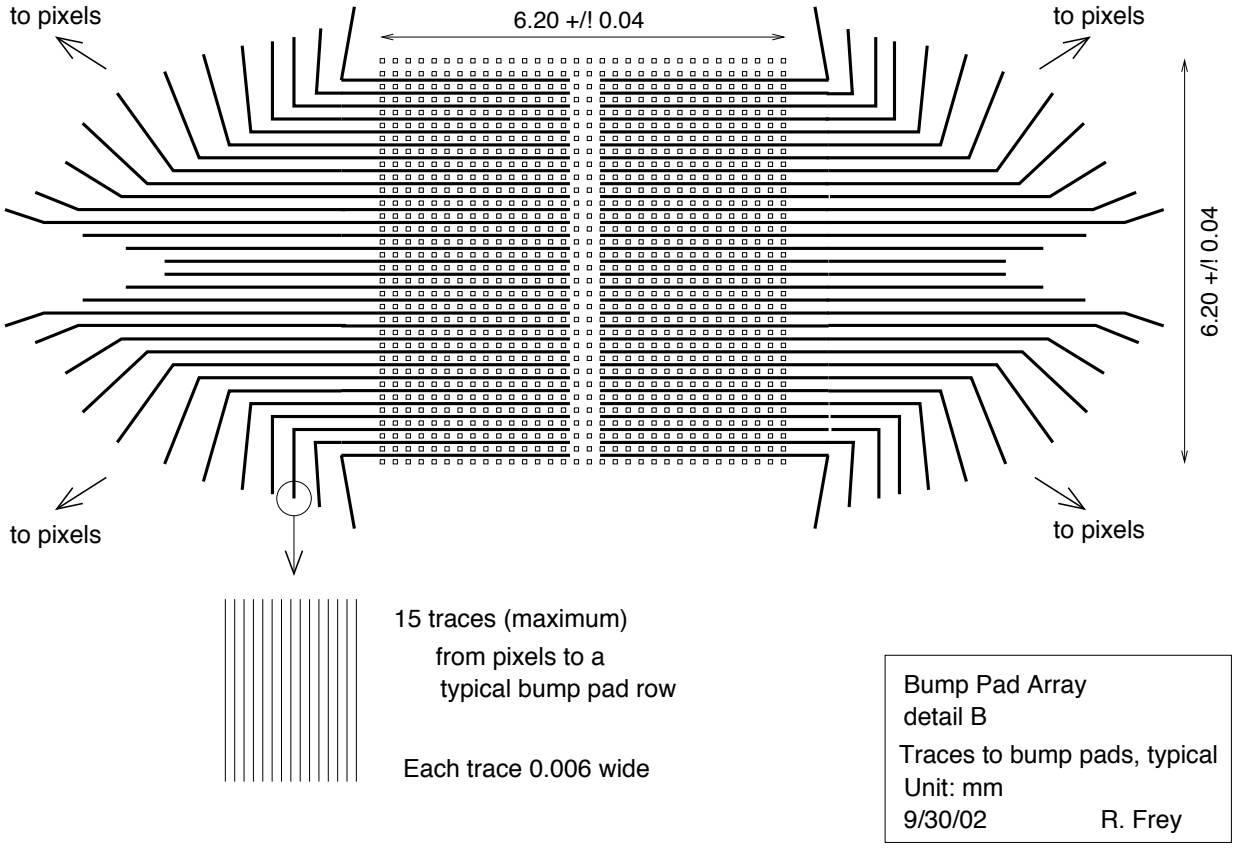
- Current in input transistor pulsed
  duty cycle $< 10^{-3}$ *0.1mW/ch*

- Currently estimating chip area and power needed for digital section



Si Prototypes

- Rough draft of design completed
  Waiting for chip area estimate to set grip spacing for bump-bonding



Si Prototype properties – leakage current and noise

• Radiation damage to detectors is probably dominated by neutrons, $\sim 10 \times 10^{10}/\mathrm{cm}^2$

$$\Rightarrow < 10\mathrm{nA} \text{ /pixel leakage current}$$

• Expect typical leakage current at start of life < 1nA/pixel

• Noise from leakage current at end-of-life for 1μ sampling time (can be adjusted) and DC coupling scheme is < 350 electrons

• Largest source of electronics noise will be front-end input transistor, noise scales as

$$\frac{C_{in}}{\sqrt{\tau} I^{1/4}} \propto \frac{C_{in}}{\sqrt{\tau} \text{power}^{1/4}}$$

• Present design has noise:

$$\sim 20 - 30 e/\text{pf}$$

For most channels the value of C_{input} is dominated by stray capacitance of the trace connecting the pixels to the electronics:

$$C_{input} \sim 5.7\text{pF(pixel)} + 12\text{pF(trace)} + 10\text{pF(amp)} \sim 30\text{pF}$$

$$\longrightarrow \sim 1000 \text{ electrons noise (c.f. 24,000 from MIP)}$$

• Analog power consumption will probably be driven by timing requirements (under investigation)

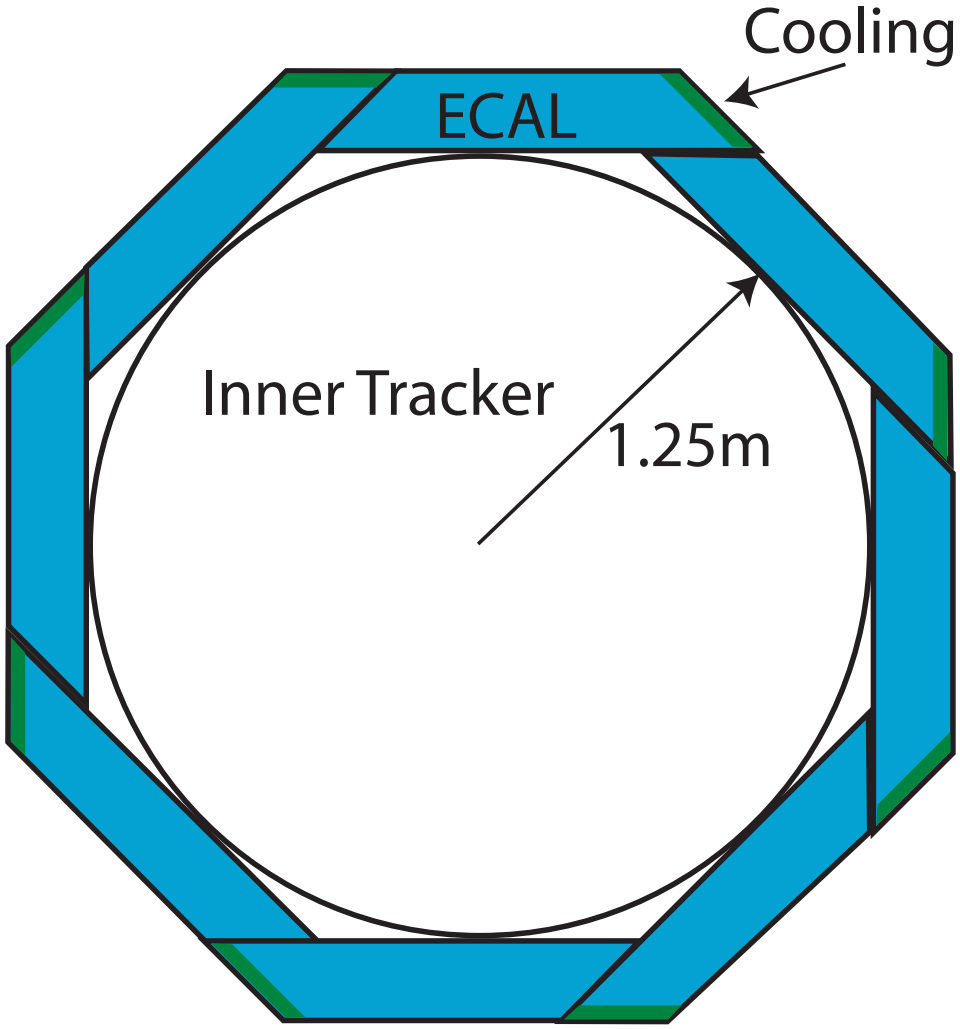
• Digital power may be dominated by drivers needed to get data off the chip

$\Rightarrow$ Data transmission schemes which minimize dissipation of heat on chip are under consideration

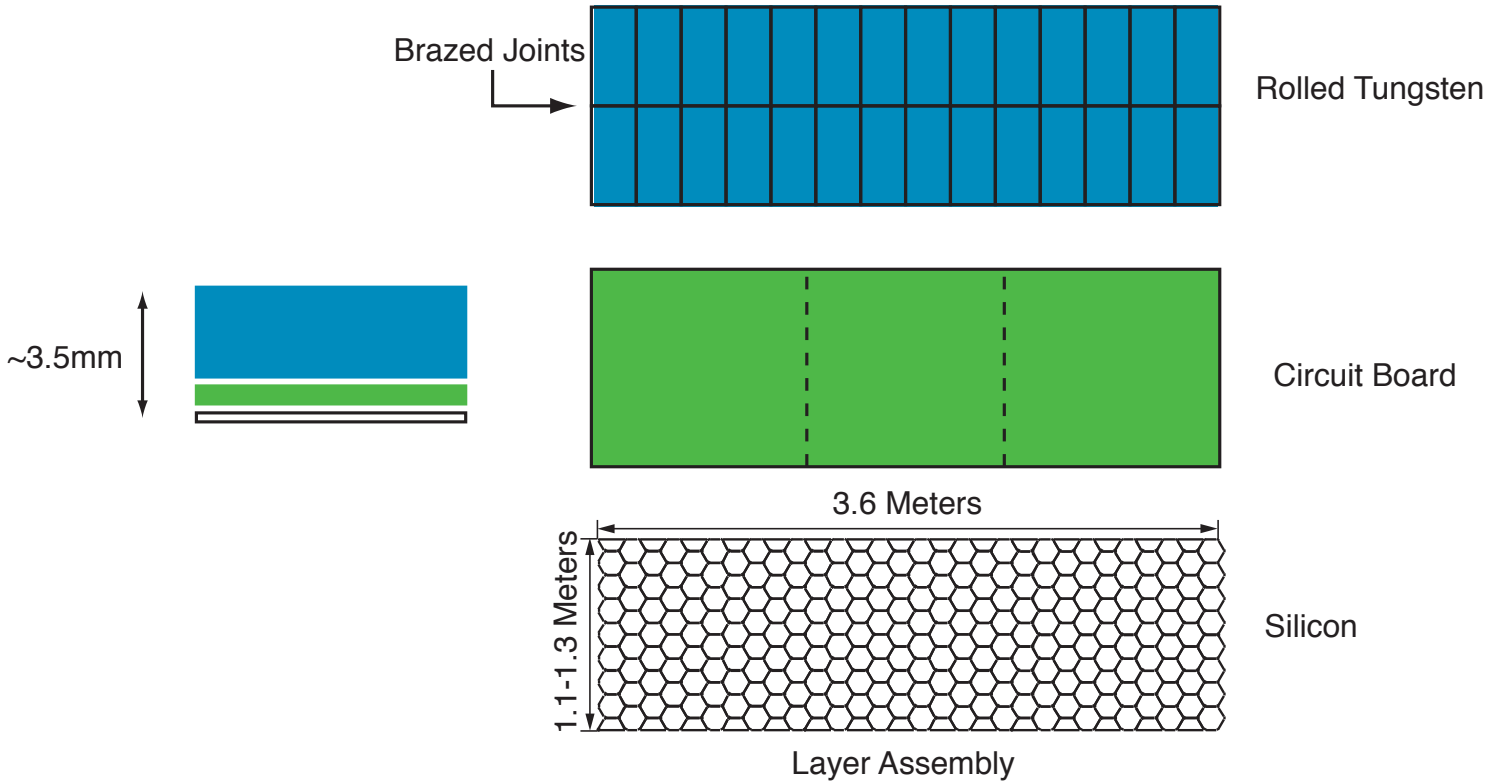
$\Rightarrow$ Maximum data rate/ chip are small $<<$ 3Mbits/s

Fitting it all together

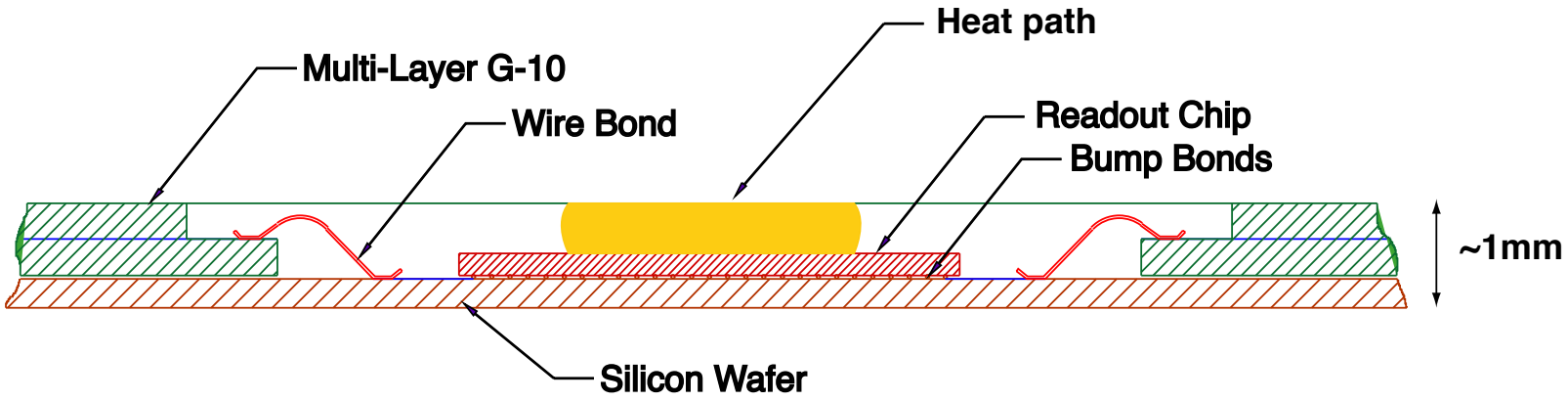
- Cartoon of possible barrel calorimeter configuration
- Assume heat flows along tungsten and/or copper heat sink to cooling water (green)
- Longest path for heat flow < 1.4m



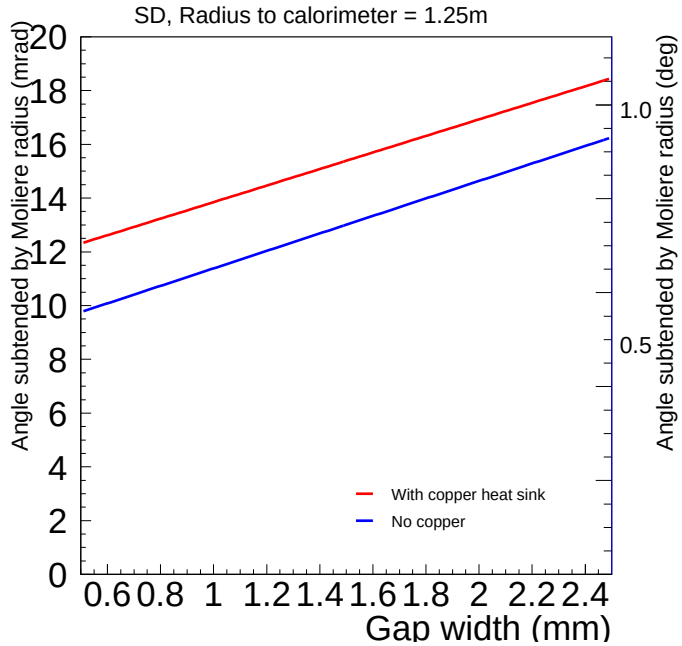
Layout of Individual calorimeter layers:



Critical parameter: minimum space between tungsten layers.



Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
+1mmCu	6.4mm	17mm



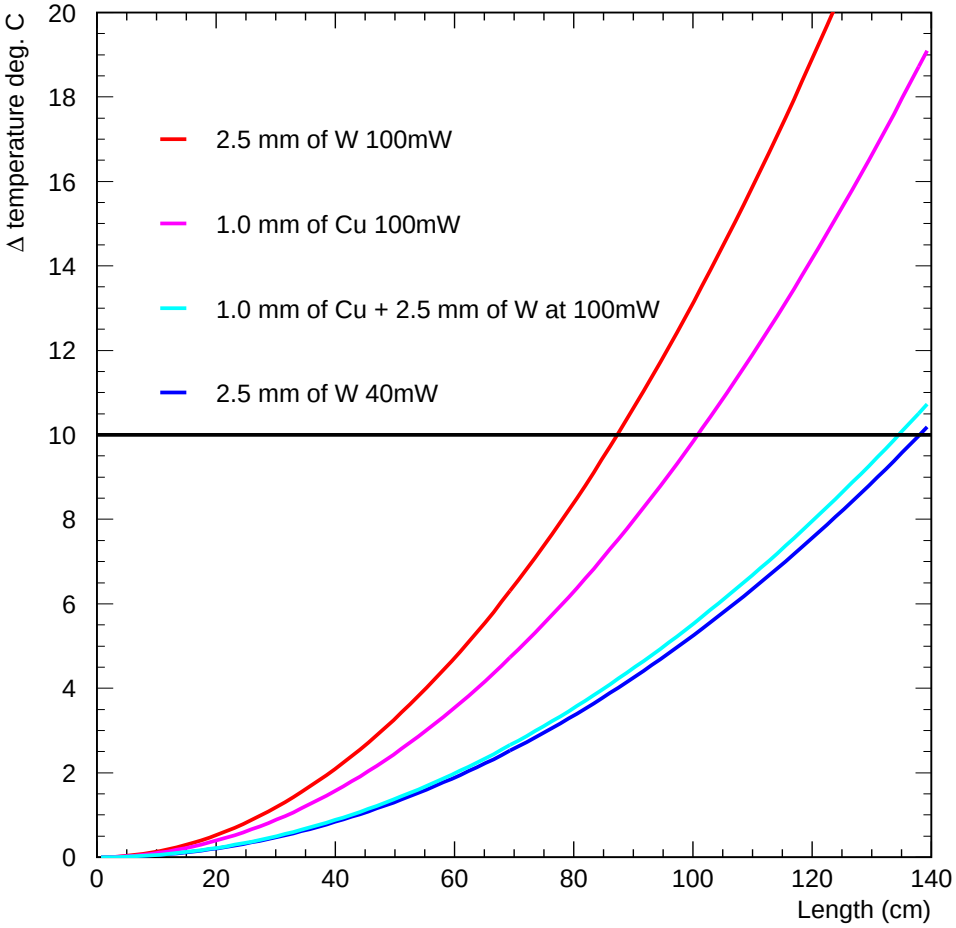
Heat flow

Back of the envelope calculation of change in temperature:

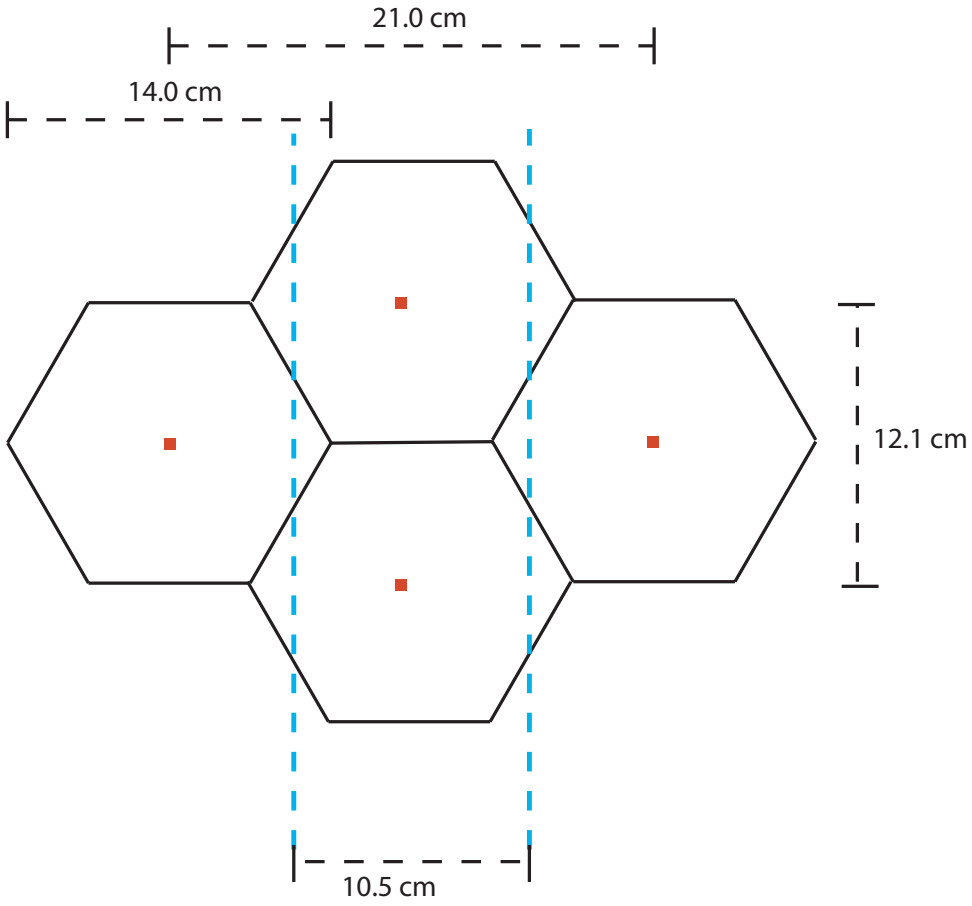
- Thermal Conductivity of W alloy 120W/(K-m)
- Thermal Conductivity of Cu 400W/(K-m)

Need to reduce heat to below 100mW/wafer.

Physical model test in progress



Model of strip of detectors equivalent to blue region:



Conclusion

- Design of silicon detectors well underway

- Electronics rough draft complete
  $\Rightarrow$ Prototypes will be ordered once area needed by the digital design is set

- Mechanical conceptual design started
  $\Rightarrow$ 1mm gap between layers without a copper heat sink may be possible
  $\Rightarrow$ Gap size depends crucially on power consumption

Near Term Plans

- Order Si prototypes – soon
- Confirm thermal model and explore best coupling method of chips to absorber
- Produce prototype electronics – next year
- Simulation, more effort needed here:
  - Optimize sampling for energy resolution
  - Optimize pixel layout
  - Would more granularity help?
  - How sensitive is energy flow to Molière radius?