Si/W_ECal Status

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Si-W Concept – SiD version

Si-W Calorimeter Concept

Transverse Segmentation ~5mm
30 or fewer long. samples
Energy Resolution ~15%/E^{1/2}
Wafer and readout chip

Multi-Layer G-10
Wire Bond
Readout Chip
Bump Bonds
Silicon Wafer

p+

n
n++

$\pm 1 \mu m$

$300 \mu m$

$\pm 1 \mu m$

$\pm 1 \mu m$
Components in hand

**Tungsten**
- Rolled 2.5mm
  - down to 1mm OK
- Very good quality
  - < 30 µm variations
- 92.5% W alloy
- Pieces up to 1m long possible

**Silicon**
- Hamamatsu detectors (10)
- Compatible with design concept for LC ECal (pixel size, traces, bump-bonding pads, etc)
- Lab tests look fine
SiD Si/W Features

- “Channel count” reduced by factor of $10^3$
- Compact – thin gap ~ 1mm
  - Moliere radius 9mm → 14 mm
- Cost nearly independent of transverse segmentation
- Power cycling – only passive cooling required
- Dynamic range OK
- Readout at pixels:
  - Low capacitance
  - Good S/N

Current configuration:
- 5 mm pixels (16 mm$^2$)
- 30 layers:
  - 20 x 5/7 X0 +
  - 10 x 10/7 X0
Beam crossing time structure

**Cold**

- 200 ms
- **Bunch trains at 5 Hz**
- **bx live: $5 \times 10^{-3}$**

- **Pileup over bunch train**
- **Or fast timing**
- **bx live: $3 \times 10^{-5}$**
- $\Rightarrow$ power pulse

**Warm**

- 8.33 ms
- **Bunch trains at 120 Hz**
- **bx live: $3 \times 10^{-5}$**

- 270 ns
- **Bunch crossings at 1.4 ns**

- **Fast readouts:**
  - OK, no pileup
  - pipeline

Electronics for a Cold LC
D. Freytag, V. Radeka, M. Breidenbach

Simplified Timing

There are ~3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
- The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
- The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
- When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output (~150 ns).
- The Track signal opens the switch lasting the sample capacitor at T0 + 1 micros. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor.
- Reset is asserted (synchronized to the bunch clock). Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event).
- The system is ready for another signal in ~12 micros.
- After the bunch train, the capacitor charge is measured by a Wilkison converter.
Frontend Design Features

• Handles full LC dynamic range while maintaining excellent S/N
  ▪ Feedback cap. switched dynamically
• Long interbunch interval (~300 ns) robustly accommodated
  ▪ Reset issued on each bx (unless a hit)
  ▪ Servo circuit to cancel leakage current integration
  ▪ Could handle reduction in bx interval to ~100 ns
• Full charge and bx time are digitized and stored in local memory on chip for the bunch train
• Power is low: <P>≈20 mW (with power cycling)
  ▪ Passive cooling should suffice
• Cold has 25X more lum. (and bkgd) per full readout cycle (train)
  ▪ Requires local storage to avoid unavailable pixels
  ▪ Current default is 4 storage cells
    • Is this enough?
    • Studies underway – Ron Cassell
    • Will the ECal have same electronics to smallest endcap angles?
• Size of one effective Moliere radius at ECal radius:
  Angle = 11 mrad
• Compare with effective Moliere radius of 3mm at 1.7m (CALICE):
  Angle = 13 mrad
⇒ The cost of the extra silicon is not put to good use.
• No longer requires large caps. – can fit within 1 mm gap
UO lab measurements of Hamamatsu prototypes

\[ C_{\text{tot}} = C_{\text{pixel}} + C_{\text{stray}} \]

\[ C_{\text{pixel}} = \epsilon A/W \]

\[ W = [2\rho \mu \epsilon V_{\text{bias}}]^{1/2} \]
Lab measurements – a typical pixel

- Cosmic rays (untriggered)
- Conventional readout

Low leakage current

Expect 22k e- for MIPs in 300 um Si
Si/W Plans

- **Next few months**
  - Complete lab detector qualification
  - Complete frontend design in 0.25 um and submit prototype run
  - Submit MRI proposal to NSF for full-depth testbeam module
    - Detectors and readout in full LC style integrated design
    - Better segmentation and Moliere radius than Calice TB module
  - LCRD proposal
    - probe some possible improvements, eg larger pixel capacitance with thicker SiO$_2$ or polyimide insulator

- **Remainder of 2005**
  - Mechanical design
  - Possible technical test beam
    - Proposal submitted for SLAC end station A – Fall 2005?
  - Prepare full TB module if funding is available
  - Simulations!
Si/W Plans (contd)

- **MRI** – test beam module
  - Silicon detectors and electronic chips for full (≈30 layers) test beam module

- **LCRD 2005** – complete basic R&D program
  - Ceramic pseudo-chip
    - Facilitate lab evaluation of detectors
    - Full analog signals for cosmic rays or SLAC test beam
  - Mechanical design and implementation
    - Mother board
    - Tungsten support
    - Cooling
  - Evaluate detector prototype(s) with thicker insulator (larger pixel capacitance)
  - Bump bonding trials (UC Davis?)